Homework Assignment 8v3
Due by bcourses submission Friday 3/24/2023 (late Monday at 9am)

1. 2020 Spring Midterm2 problem 8
2. With respect to the op-amp in that bandgap reference circuit, we want to figure out which topologies would work. Assume process parameters from our “particular technology” given below, and a supply voltage consisting of two alkaline batteries in series (3.2V fresh, 1.6V at end of life). Assume that the current source transistors (whose gates are connected to the output of the op-amp) have an overdrive voltage of 200mV.
   a. What is the input common mode voltage on the op-amp at room temperature? Does that prevent us from using NMOS input differential pairs or PMOS input differential pairs?
   b. What is the output voltage that is needed if VDD=1.6V? Can a PMOS 5T op-amp supply that output voltage at the common mode from part a?
   c. Same question, but for VDD=3.2V.
   d. Can a PMOS-input current mirror op-amp meet both the input common mode and output swing requirements at room temperature over the supply voltage range? Can any other op-amp topology that we have studied meet the input/output requirements?
   e. What is the required input common mode range over the industrial temperature range [-40C,+85C]?
   f. What are NMOS and PMOS threshold voltages over that same temperature range? Assume that their temperature coefficients are -2mV/K and +2mV/K respectively.
   g. What is the output swing needed as a function of VDD over that same temperature range? Consider the current sources being driven by the op-amp, and both the temperature coefficient of their threshold voltage, and the difference in current that they need to drive at different temperatures.
   h. Carefully plot your answers above vs. temperature. Input common mode, thresholds, and output swing at VDD=1.6 and 3.2V
   i. Which op-amp topologies will work over the entire voltage and temperature range?
3. For the two circuits below, assume that all transistors are in quadratic saturation and that gmro>>1 to simplify your answers.
   a. Draw an arrow on each device showing the positive direction for Id to avoid confusion on sign conventions.
   b. For the Gm calculation, does the value of RUP matter? Why or why not?
   c. Make a table with one column for each circuit, and the following rows: Id3, Gm, Ro. Calculate Id3 in terms of Id1 and Id2, and Gm, Ro in terms of gm and ro for M1-3.
4. In a particular technology $C_{ox}=10fF/um^2$, $C_{ov}=0.5fF/um$, $\mu_nC_{ox}=250\mu A/V^2$, $\mu_pC_{ox}=50\mu A/V^2$, $\lambda=0.18um/(L*5V)$, $V_{tp}=V_{tn}=0.6V$.

For the PMOS-input folded cascode op-amp below, assume the quadratic model.

![Circuit Diagram]

a. Calculate and tabulate:
   i. the overdrive voltage and current in all devices. For this step you may assume that $\lambda=0$. The simplest order may be Mb1 through Mb6, then M1 through M5 in order.
   ii. Calculate the bias voltages on all nodes, assuming $V_{CM}=0V$. Specifically: tail, G2, G3, G6, G5, G4, S3B, S4AB, and out.
   iii. The region of operation of all devices (off, sub-thresh, linear, saturation)
   iv. the $g_m$ and $r_o$ parameters for M1 through M5

b. Calculate $Gm$, $Ro$, and $Av$

c. Calculate the input common mode range and output swing.

d. What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing? How would you change the size of Mb5 to achieve that voltage?

e. If the load capacitance is 1pF (roughly the same as the input capacitance),
   i. What are the frequencies of the pole/zero doublets from the current mirror?
   ii. what are the pole and unity gain frequencies?
   iii. What is the phase margin in unity gain?