Homework Assignment 6
Due by bcourses submission Friday 3/10/2023 (late Saturday at 9am)

1. Take a look at the LM324 datasheet again.
   a. From the schematic, estimate the common mode input range. What is the input common mode voltage range quoted in table 6.5? Do your answers agree?
   b. From the open loop gain, and the gain-bandwidth product, estimate the location of the dominant pole. Compare to the 135 degree phase extrapolated from Figure 6-6. Are they close?
   c. From the slew rate in figure 6-32 and the tail current source, estimate the size of the compensation capacitor.

2. Some solutions to last week’s 2-stage op-amp design used $v_{ov}=100$ mV for all devices. The gain of the first stage is then 50
   a. What is the change in the output of stage1 that is needed to turn M4 off?
   b. What is the differential input needed to get that output change?
   c. With a capacitive load of 1 pF at the output and a differential input sufficient to turn M4 off, what is the rate of change of the output voltage while M5 remains in saturation? Will the output voltage go all the way to zero?
   d. With a capacitive load of 1 pF at the output and a differential input sufficient to double the overdrive voltage on M4, what is the rate of change of the output voltage while M4 remains in saturation? Will the output voltage go all the way to $V_{DD}$?

3. Check out the datasheet for the K2-W tube op-amp. This op-amp, released in 1952, was the first production op-amp. It runs from a +/-300V supply, and has a bandwidth of 300kHz (or k-cycles/s, as they said back then – the unit Hertz not having been established yet). There’s a schematic on page 2. (You may want to draw the circuit with NMOS FETs instead of tubes to help you figure it out.) Pins 1, 2, and 6 on the bottom of the figure are $V+$, $V-$, and $V_{out}$. VR1 and VR2 are neon bulbs that provide a low impedance level shift of roughly 100V to center the output between the rails. Identify (circle and label)
   a. input differential pair
   b. diff-pair load resistor
   c. tail current resistor.
   d. Estimate the common mode gain and write it near the tail resistor.
   e. Common-cathode gain stage (like CS or CE)
   f. Cathode-follower output stage (like source-follower or emitter follower, CD, CC)
   g. Miller-multiplied compensation capacitor from the output back to the input of the gain stage.
   h. Bonus points if you can identify positive feedback in this amplifier, designed to increase the low-frequency gain (which ended up at about 20,000).

4. You have three op-amp topologies: single stage active load (our standard 5 transistor opamp), the two stage version of that, and the current mirror op-amp. Each topology can either have NMOS or PMOS inputs, for six different op-amps. For each of the PMOS versions only, sketch the op-amp schematic, and sketch the output swing vs. common mode input range.
5. You have an op-amp with a low-frequency gain of 1,000,000 and a single pole at 1 krad/s. Plot the location of the pole as a function of the feedback factor $f$ from $f=0$ to 1. Now with $f=0.1$

   a. Sketch the Bode plot of the closed-loop amplifier

   b. What is the fractional gain error at low frequency?

   c. What is the time constant of the step response? How does it compare to the open-loop time constant?

   d. What is the unity gain frequency? How does it compare to the open-loop unity gain frequency?

6. You now have an opamp with a low-frequency gain of 1,000,000 and three poles at 1 krad/s.

   a. Plot the location of the three poles as a function of the feedback factor $f$.

   b. At the point where the poles cross the jw axis, annotate the plot with the value of $f$ that gives this pole location.

   c. Using this value for $f$, draw a Bode plot of the loop gain $A_f$

7. A two-stage CMOS op-amp running at a particular bias point has the following parameters: $G_{m1}=0.1\text{mS}$, $R_{o1}=10\text{M}$, $C_1=0.1\text{pF}$, $C_c=0\text{pF}$, $G_{m2}=1\text{mS}$, $R_{o1}=100\text{k}$, $C_2=100\text{pF}$.

   a. Plot the magnitude and phase of the overall gain of this uncompensated amplifier.

   b. Where are the poles of the uncompensated amplifier? Is it unity-gain stable?

8. For the same amplifier as above, we now add $C_c=1\text{pF}$. For this problem, you may ignore the RHP zero that this introduces.

   a. Plot the magnitude of the second stage gain vs. frequency

   b. Plot the magnitude of the input capacitance of the second stage (including $C_c$) vs. frequency

   c. Plot the magnitude of the input impedance of the second stage vs. frequency. Add a line for the output impedance of the first stage.

   d. Now plot the magnitude of the gain of the first stage on the top plot, and the magnitude of the overall gain of the amplifier

   e. What are the compensated poles of the amplifier? If $C_c$ were 0, where would the poles of the amplifier be?

9. [not graded] For a standard 5 transistor CMOS differential amplifier show that the gain from a differential input to the (so called virtual ground!) tail voltage is $1/4$. You can assume that $g_{m}r_0 \gg 1$ for all combinations of $g_m$ and $r_0$. You can win bets with experienced IC designers with this knowledge!