Key

EECS140 Final
Fall 2019

Name Good Luck, Have Fun!

SID top secret

Prob.	Score
1	/~~10~~
2,3	/20
4	/16
5	/16
6	/~~20~~ 21
7	/8
8	/15
9	/14
10	/10
11	/15
12	/22
Total	/165

for q1: All points for correct procedure, no #'s for this one...

1. [8] The I-V curves below are from an Indium Gallium Zinc Oxide transistor used in flat panel display TVs.

2 a. Estimate g_m when V_{GS}= 10V and V_{DS}= 10V. Write down what ΔI and ΔV you are using for your calculation.

$g_m \triangleq \frac{\Delta I}{\Delta V}$, for $\Delta V = 2.5V$, $\Delta I \approx 0.06 - 0.02 \approx 0.04mA$

$= \frac{0.04mA}{2.5V}$

2 b. Estimate $g_o=1/r_o$ under the same conditions. Draw the line that you are using to estimate g_o. Say slope $\approx \frac{0.01mA}{10V} \approx \frac{0.001}{V} = g_o$

2 c. Calculate the intrinsic gain from parts a and b

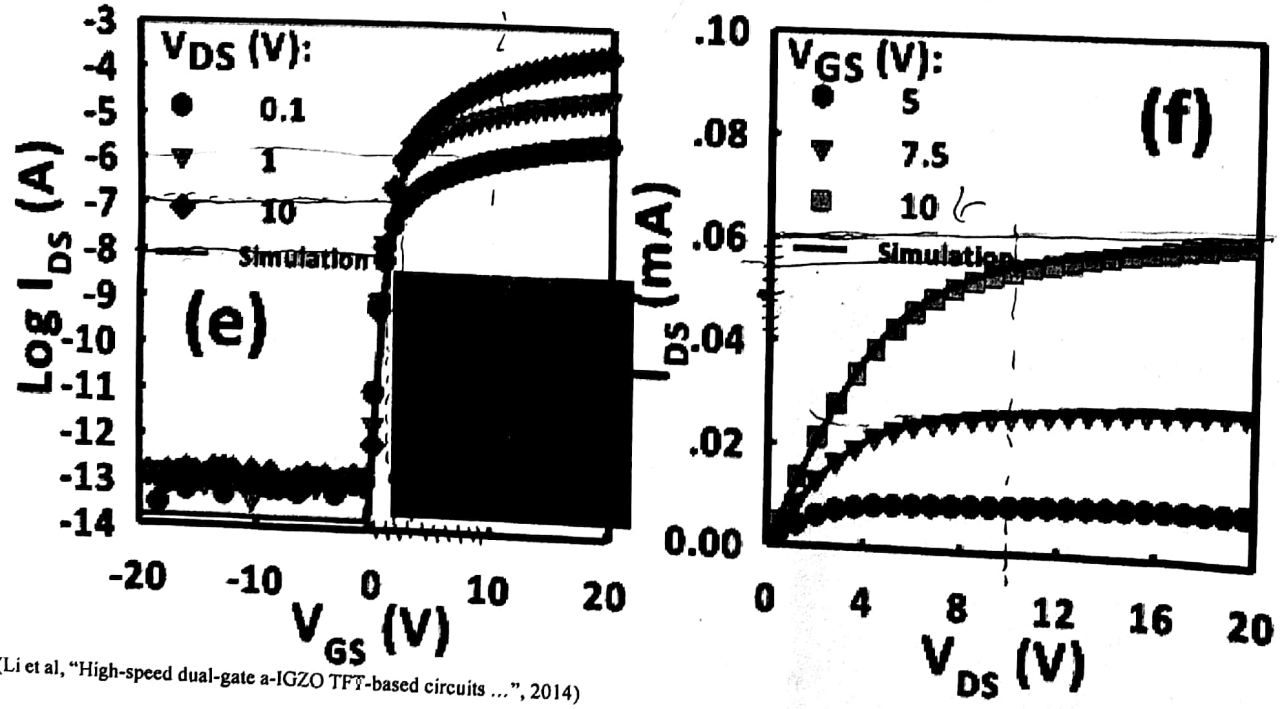
$\frac{0.04mA}{2.5V} \cdot \frac{10}{0.01mA} = \frac{0.4}{2.5 \cdot 0.01} = \frac{40}{2.5} = 16$

2 d. If I_{DS}=10nA when V_{GS}=2V, estimate the sub-threshold slope.

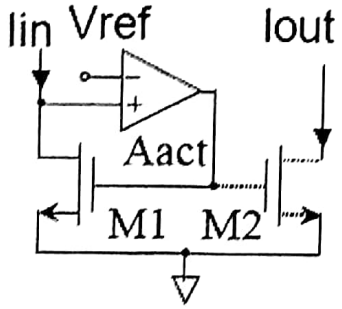
10nA => −8 on a $\log_{10}$ scale

0V ≈ −13

So ~ 5decades/2V ≈ 100

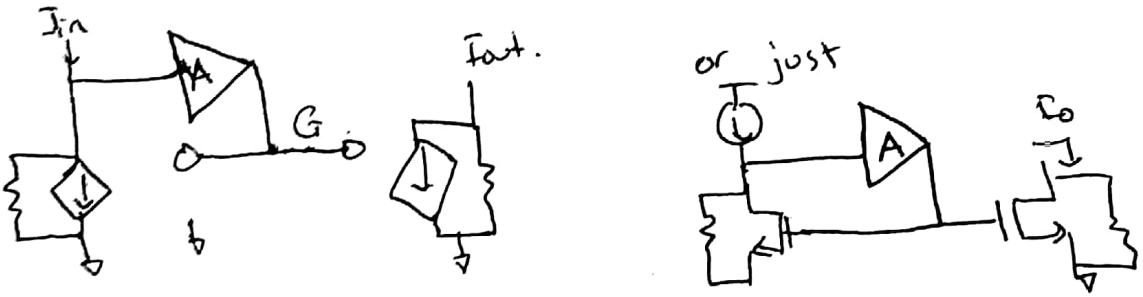


(Li et al, "High-speed dual-gate a-IGZO TFT-based circuits ...", 2014)



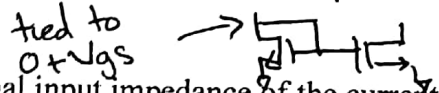
2. [10] For the current mirror shown here,

1 a. Draw the small signal model of the circuit, assuming that the amplifier is an ideal op-amp with a large positive gain A, and that V_{ref} is a constant voltage.



3 b. What is the minimum value of Vref for which transistor M1 will remain in saturation? If we compare this circuit to a typical simple current mirror, which has a lower minimum input voltage? Why?

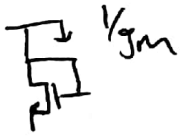
Vref > V_{ov1}, which is lower than the simple mirror.



4 c. Write an expression for the small-signal input impedance of the current mirror. How does that compare to a simple current mirror?

(actual answer is $\frac{r_{o1}}{1+g_{m1}r_{o1}A}$)

$R_i \approx \frac{1}{g_{m1}A}$ compare to



2 d. Write an expression for the output impedance of the current mirror

$R_o = r_{o2}$ nothing new here

3. [10] You are designing a single-stage CMOS op-amp to be used in feedback to achieve a gain of 5. The gain must be accurate to 1% from DC to 1 Mrad/s (including any 3dB losses). The load is a 10pF capacitor. You are restricted to biasing your transistors with overdrives between 100mV and 1V, and they look reasonably quadratic in that range.

$f = 1/5$

4 a. What is the minimum open-loop gain and dominant pole location of the op-amp?

$\frac{1}{A_f} \cdot 0.01$, $A = \frac{1}{[1\% \cdot f]} = 5 \cdot 100 = 500$.

$\omega_p \approx 1$ Mrad/s

2 b. What is the minimum unity gain frequency of the op-amp?

$\omega_u = GBW = 500 \cdot 1$ Mrad/s $= 500$ Mrad/s

2 c. What is the minimum transconductance of the input transistors?

$\omega_u = g_m/C_L \Rightarrow g_m = 500\text{M}\frac{\text{rad}}{\text{s}} \cdot 10^{-11}\text{F} = 10^{-3}\text{S} \cdot 5$

2 d. What is the minimum current in each of the input transistors?

$g_m = \frac{2I_D}{V_{ov}}$, say $V_{ov} = 100\text{mV}$, then $\frac{2I_D}{0.1} = 10^{-3}$

$I_D = 5 \cdot 10^{-4}/2\ \text{A} = 250\ \mu\text{A}$

[16] For the figure below you may assume that the switches and op-amp are ideal. ϕ_1 and ϕ_2 are non-overlapping clocks. Assume all of your capacitors are initially discharged.

a. After the first round of ϕ_1 and ϕ_2 (we'll call it cycle 0), what is the charge, $Q_F[0]$, on the right side of C_F in terms of that cycle's input, $V_{IN}[0]$?

$Q_S[0] = Q_X[0] = C_S(0 - V_{IN}[0]) = C_F(0 - V_{OUT}[0]) = -Q_F[0]$ $\quad \boxed{Q_F[0] = C_S V_{IN}[0]}$

b. What is the corresponding voltage, $V_{OUT}[0]$?

$$\boxed{V_{OUT}[0] = \frac{C_S}{C_F} V_{IN}[0] = \frac{Q_F[0]}{C_F}}$$

c. Now the input voltage has changed to $V_{IN}[1]$. What is the charge $Q_F[1]$ on the right side of C_F after the next cycle in terms of $Q_F[0]$ and $V_{IN}[1]$?

$Q_S[1] = C_S(-V_{IN}[1])$

$Q_X[1] = Q_X[0] + Q_S[1]$ $\rightarrow$ $Q_F[1] = Q_F[0] - Q_S[1]$

$\boxed{Q_F[1] = Q_F[0] + C_S V_{IN}[1]}$

d. Write an expression for $V_{OUT}[n]$, the output voltage after n cycles.

$$V_{OUT}[n] = \frac{Q_F[n]}{C_F} = \frac{C_S}{C_F} \sum_{i=0}^{n} V_{IN}[i]$$

e. What do we call this kind of circuit?

integrator

Same circuit, different types of questions:

f. During ϕ_2 what is the feedback factor for the amplifier?

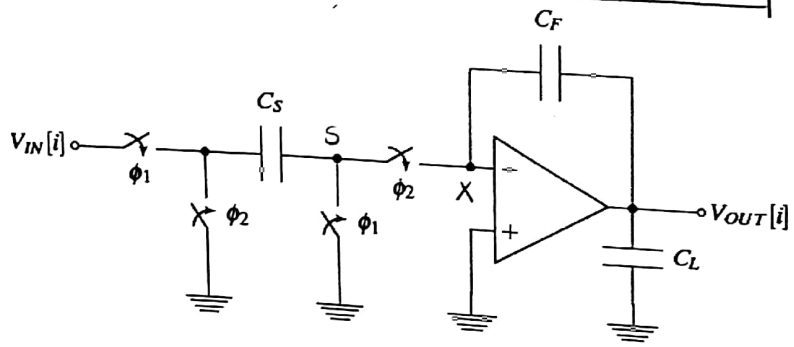
$$\boxed{f = \frac{C_F}{C_S + C_F}}$$

g. During ϕ_2 what is the total capacitance at the output of the amplifier?

$$\boxed{C_{total} = C_L + (1-f) C_F}$$

h. If there is parasitic capacitance Cp on node V-, does that change the feedback factor during ϕ_2, and if s what is the new feedback factor?

$$\boxed{f = \frac{C_F}{C_F + C_S + C_P}}$$



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5 — [15] Given the cascode amplifier below, g_m=1ms and r_o=10k. C_L=2pF, C_{gs}=100fF and you may assume that all other capacitors are zero. The current source has an output impedance of 1M.

a. On the next page, plot the magnitude of the output impedance, Z_{out}, vs. frequency. LABEL AXES CLEARLY (3pts)

$Z_o = g_m r_o^2 \,\|\, 1M = 10^{-3} \cdot 10^8 \,\|\, 1M \approx 10^5$

b. What is the output pole frequency? (1pt)

$$P_L = \frac{1}{10^5 \cdot 10^{-12} \cdot 2} = \frac{1}{5\cdot 10^{-7}} = 5M \text{ rad/s}$$

c. What is the low frequency impedance seen looking into the source of M2? (2pts)

$$\frac{1}{g_{m_2}}\left(1+\frac{R_d}{r_o}\right) = 10^3(1+100) \approx 10^5\,\Omega$$

(R_d = 1MΩ, r_o = 10^4)

d. What is the low frequency gain from V_{in} to the drain of M1? (1pt)

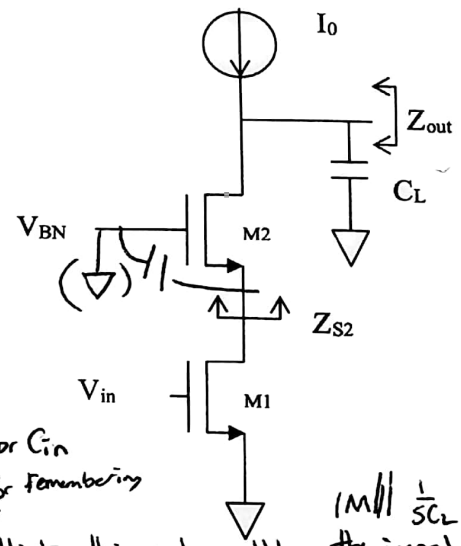
$$\left| g_{m_1} \cdot (r_{o1} \,\|\, Z_{S2}) \right| \approx 10^4 \cdot 10^{-3} = -10 \text{ V/V}$$

e. What is the low frequency input capacitance if C_{gd}=20fF? (2pts)

Miller Cap! $C_{gd}(1+10) = 220fF$. Add C_{gs} for C_{in}

$C_{in} = 220fF + 100fF = 320fF$

all pts for remembering miller cap!



f. Plot the magnitude of the impedance looking into the source of M2, Z_{S2}, vs. frequency. LABEL AXES CLEARLY (6pts, 2 per pole/zero)

Multiple things here!!! $1M \,\|\, \frac{1}{sC_L}$ is the impedance Z_d, seen drain of M_2

$$Z_{S2} = \frac{1}{sC_{gs_2}} \,\|\, \left[\frac{1}{g_m}\left(1+\frac{(1M \,\|\, 1/sC_L)}{r_{o_2}}\right)\right]$$

g) What is the second pole frequency? (1pt)

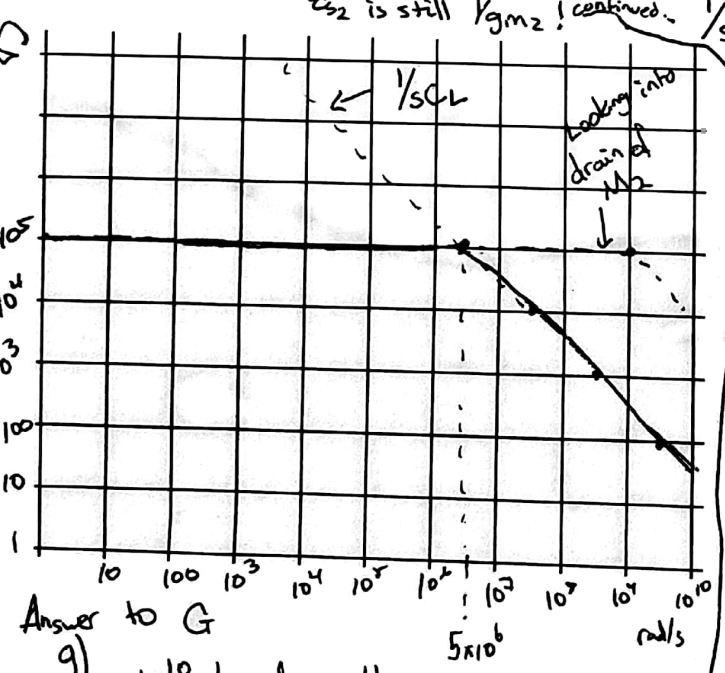
What's the dominant pole?

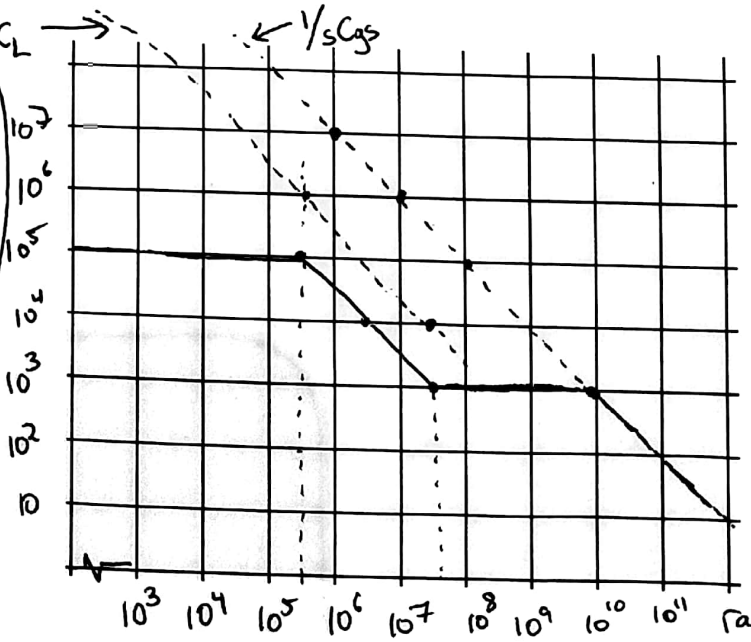
Note Z_d will roll-off when $\frac{1}{sC_L} = 1M\Omega$, @ $s = 5\times10^5$ rad/s. At this frequency $\frac{1}{sC_{gs_2}}$ is still very large, & so is inconsequential.

But wait, there's more! There is a zero! recall $Z_{S2} = \frac{1}{g_{m_2}}\left(1+\frac{R_d(s)}{r_o}\right)$,

Magnitude of Z_{out} so when $Z_d(s)/r_o \ll 1$, Z_{S2} is still $1/g_{m_2}$! continued...

Magnitude of Z_{S2}





Answer to G

9) 10^{10}, based on the plot (intersection of $1/sC_{gs}$ loadline) (1pt)

$\therefore$ Zero @ $1 = \frac{R_d(s)}{r_o}$ or when $Z_d(s) = r_o$

This is when $\frac{1}{sC_L} = 10^4$, @ $s = 5\cdot10^7$ rad/s

[20] For the figure below, Vtn=-Vtp=1V. The overdrive voltage on M5 and M7 is 100 mV. You may ignore body effect, and assume that the devices all look quadratic.

a. Assuming lambda=0, estimate the currents in on the transistors in the table below

b. Assuming lambda=0, estimate the bias voltages on the gates of the transistors in the table below

The square root of 20 is approximately 4.5

each

	M1	M3	M5	M7	M9	M11	M16	M17
$\|I_D\|$	100 uA	200 uA	200uA	200uA	200 uA	100 uA	100 uA	200 uA
V_G	3V	3.9V	3.9V	1.1V	1.1V	1.45V	3.9V	3.55V

c. Estimate the input common mode range (give a voltage for each)

2 each

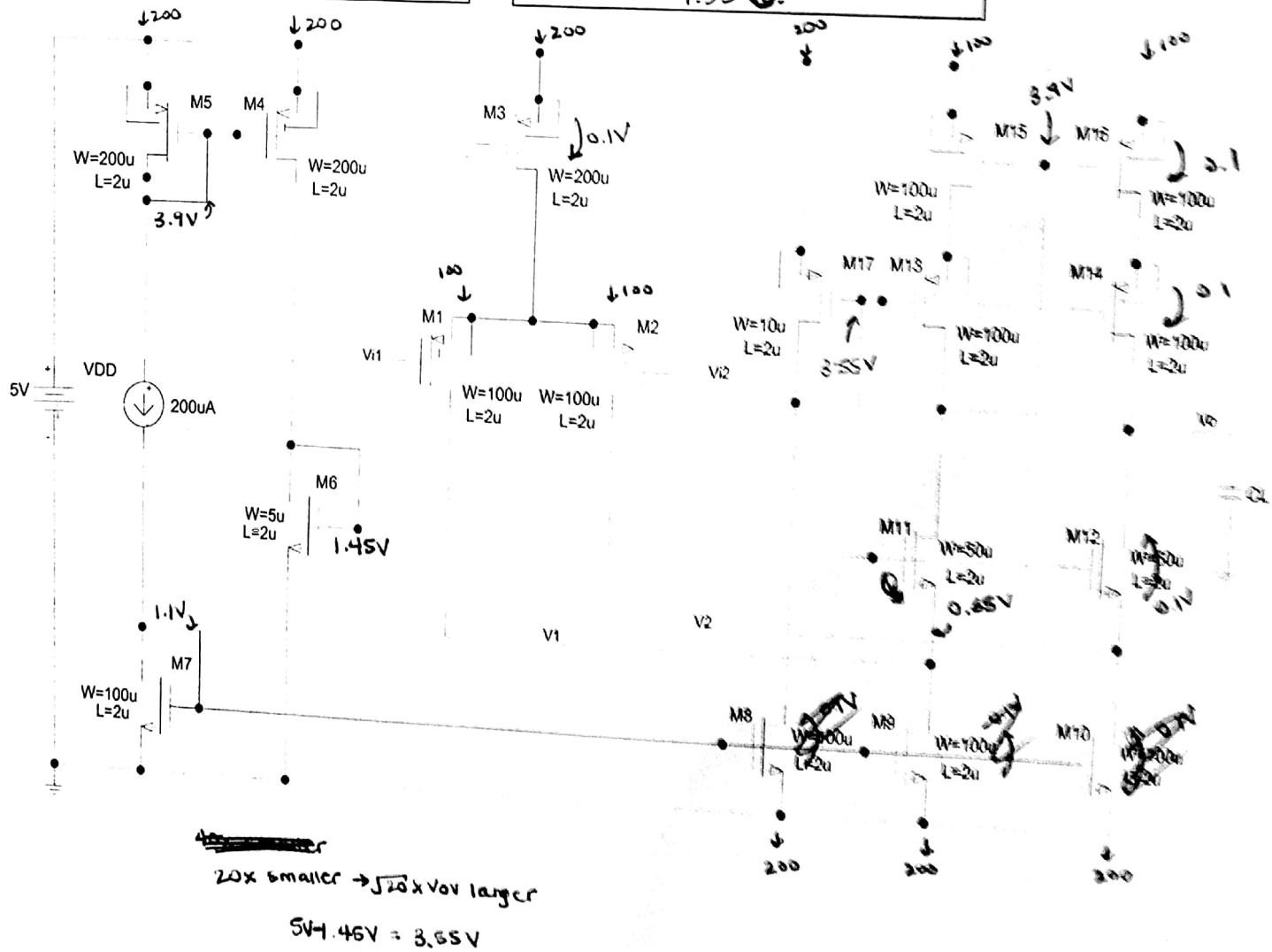
$V_{icm,\,min}$ = ~~[redacted]~~ 0.65

$V_{icm,\,max}$ = ~~[redacted]~~ 3.8V

d. Estimate the output swing for which all transistors will remain in saturation

$V_{o,\,min}$ = ~~[redacted]~~ 0.45V

$V_{o,\,max}$ = ~~[redacted]~~ 4.55



~~[redacted]~~ 20x smaller → $\sqrt{20}$ x Vov larger

5V-1.46V = 3.55V

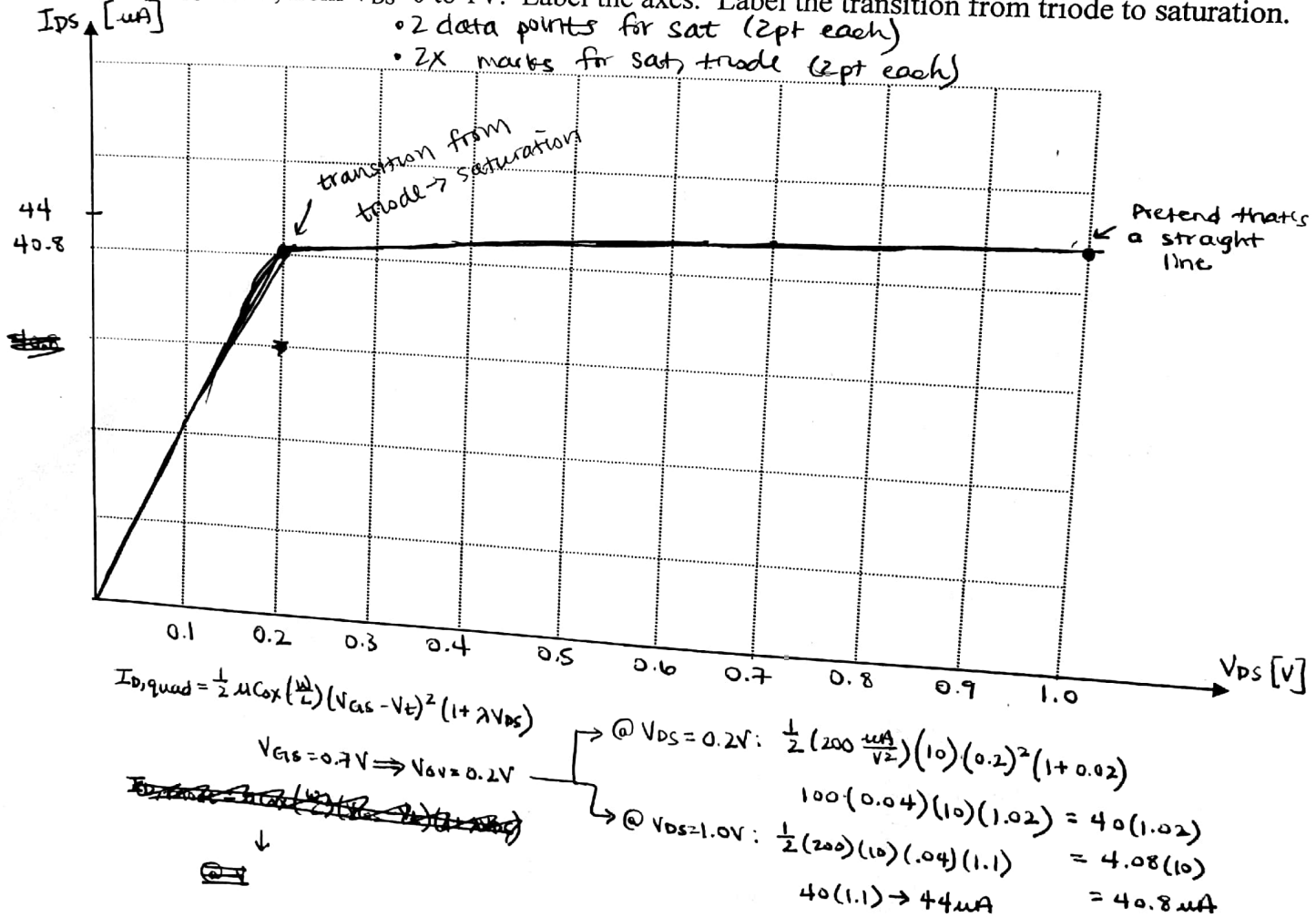
For the following problems related to the project, you will be working in a CMOS process with $\mu_n C_{ox}$=200uA/V^2, $\mu_p C_{ox}$ =100uA/V^2, V_{tn}= -V_{tp}= 0.5Vand λ = 1/(10V) (1um/L) with W_{min}=L_{min}=1um. Note that this is NOT the same process as you used for your project this semester.
The supply is 2 alkaline cells, so V_{bat} = 1.6..3.2V

You will design parts of the following analog blocks

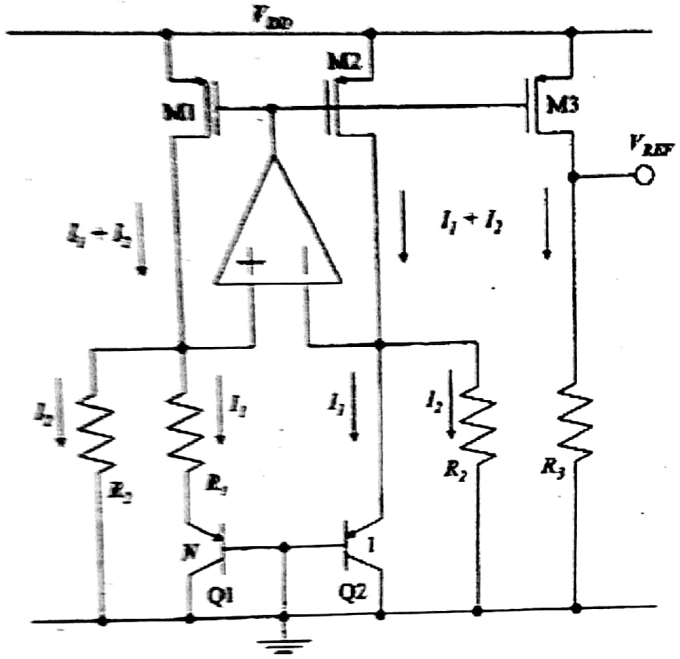
- A low voltage bandgap reference
- an analog regulator with an output of 1.25 V
- an ADC reference voltage of 1V
- a digital regulator with an output of 1.5 V
- a 2-input analog multplexor with a single control bit
- a programmable gain amplifier with one gain select bit, and a gain of either 1 or 5
- a 10 bit switched capacitor ADC. **The ADC has an input range from 0-1V.** This is less than V_{DDA}.

op-amp topologies for parts "b" below: N or P input; 5 transistor, current mirror, 2 stage, folded cascode

7. [8] To get started, carefully sketch the drain current vs. drain voltage for an NMOS transistor with W/L=10u/1u, V_{GS}=0.7V, from V_{DS}=0 to 1V. Label the axes. Label the transition from triode to saturation.



Low-voltage Bandgap



For the above circuit, assume that the op-amp is high gain and the transistors are identical with high output impedance

2 a) Explain why (prove) the three currents labeled "I_1+I_2" must be equal, why the two currents labeled I_2 must be equal, and why the two currents labeled I_1 must be equal.

$V^+ = V^-$, & $I_2 = V^+/R_2$ for both sides.

I_1+I_2 is equal both sides due to mirror M1 & M2

I_1 equal both sides due to above (algebra)

2 b) What is the voltage across R_1?

$\Delta V_{be} = \ln(N) \cdot V_{thermal}$

2 c) Write expressions for I_1 and I_2 in terms of V_{eb2} (the right diode voltage), V_{th} (thermal voltage), R1, N, and R2.

$I_1 = \frac{\Delta V_{be}}{R_1}$, PTAT

$I_2 = \frac{V_{EB2}}{R_2}$

2 d) For I_1 and I_2, which one is PTAT, which one has a negative temperature coefficient?

I_1 PTAT I_2 CTAT

2 e) Put it all together: Find the equation for V_{ref}!

$V_{ref} = (I_1+I_2)R_3 = \frac{R_3}{R_2}\left(V_{eb2} + \left(\frac{R_2}{R_1}\right)\ln N \cdot V_{th}\right)$

2 f) Roughly what should the ratio between R_1 and R_2 be to get zero temperature coefficient on V_{ref}? Write one as an integer times the other. if $V_{be} \approx -2mV/K$, $V_{th} \approx +0.085mV/K$

$\frac{R_2}{R_1} = \frac{+2mV/K}{0.085mV/K \cdot \ln(N)}$

2 g) Roughly what should the ratio between R_2 and R_3 be to get V_{ref}=0.6 V? Write one as an integer times the other. Bandgap $\approx 1.2V$.

So $R_3 = \frac{1}{2}R_2$ or $\frac{R_3}{R_2} = \frac{1}{2}$

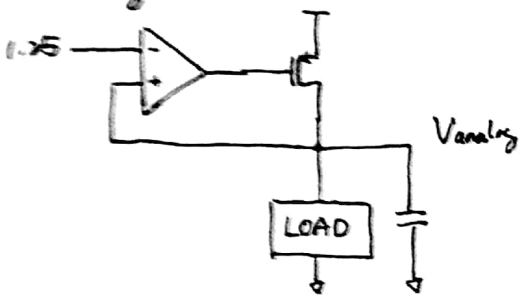
1 h) Give the minimum required supply voltage for this circuit if the mirror transistors have a V_{ov} of 200mV and V_{eb2} = 0.65V.

0.85V

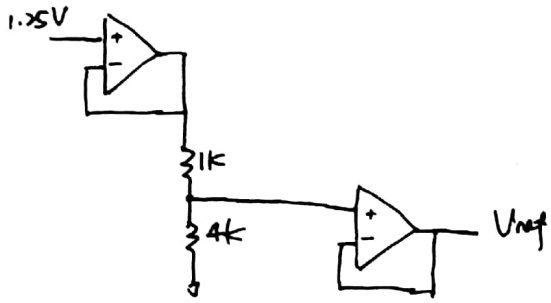
Regulators. You decide not to use the fancy low-voltage bandgap, and go back to a traditional one.

a. [9] draw the schematic for the analog regulator (1.25V), digital regulator (1.5V), and ADC reference regulator (1V) using op-amp symbols, assuming that the bandgap is producing V_{BG}=1.25V. If you use resistors, clearly indicate what their ratios should be.

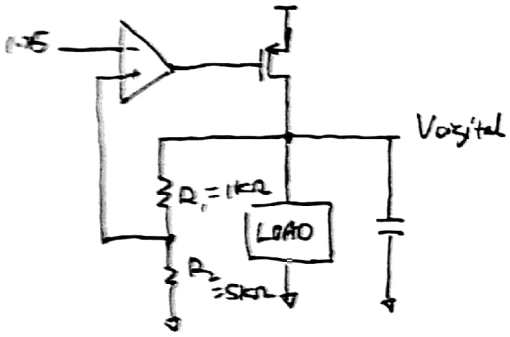
Analog



ADC reference:



Digital



$V_{digital}$ (1.5) $\cdot \frac{R_2}{R_1+R_2} = 1.25$

$R_1 : R_2 = 1:5$

$R_1 = 1K\Omega$, $R_2 = 5K\Omega$

b. [5] for the digital regulator op-amp:

i. what is the common mode input?

1.25V

ii. what is the output swing needed?

$V_{DD} - V_{th} - V_{ovp} \approx V_{DD} - V_{th}$

iii. what is the voltage supply?

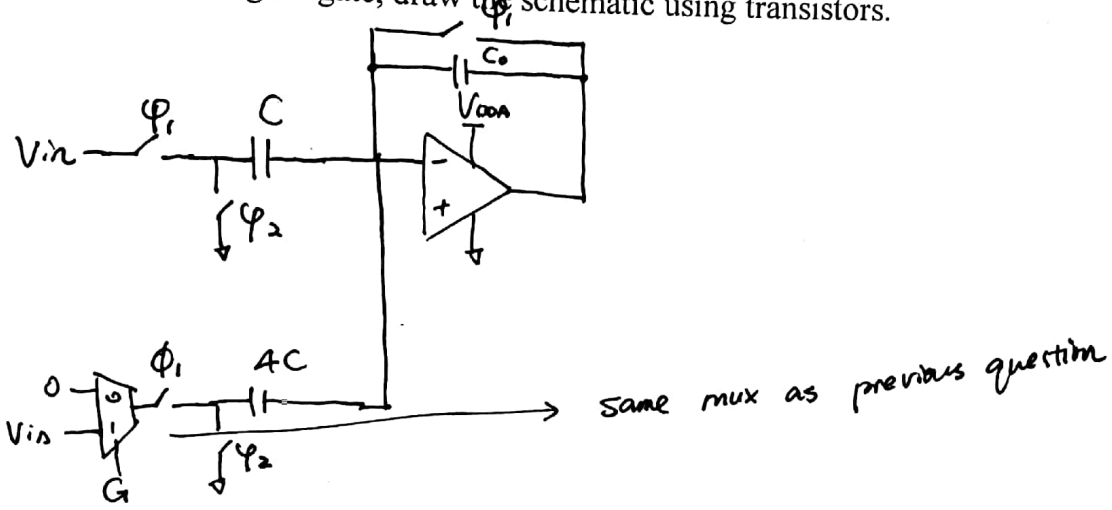
1.6V - 3.2V

iv. which topologies will NOT work, and why?

- Pmos input will not work

Gain of 1 or 5 PGA

a. [10] draw the schematic using an op-amp symbol, transistors, and capacitors. Assume that the gain control bit G and two non-overlapping clock phases ϕ_1 and ϕ_2 are in the analog power domain (0, V_{DDA}). If you need a digital gate, draw the schematic using transistors.



b. [5] for the op-amp:

i. what is the common mode input?

0V

ii. what is the output swing needed?

iii. what is the voltage supply

0 - V_{DDA} or 0 - V_{DDnof}

V_{DDA}

iv. which topologies will NOT work, and why?

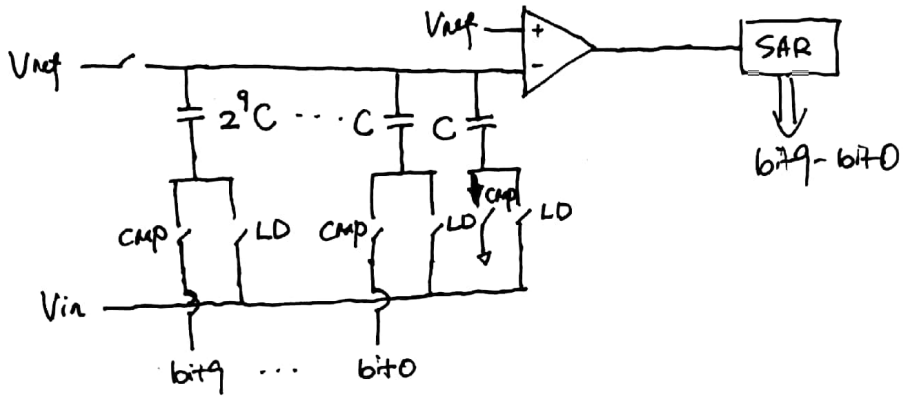
1) NMOS input not work

2) 5T

3) without a output stages

ADC. Vin=0 to 1V. The reference voltage is 1V. The analog supply is 1.25 V.

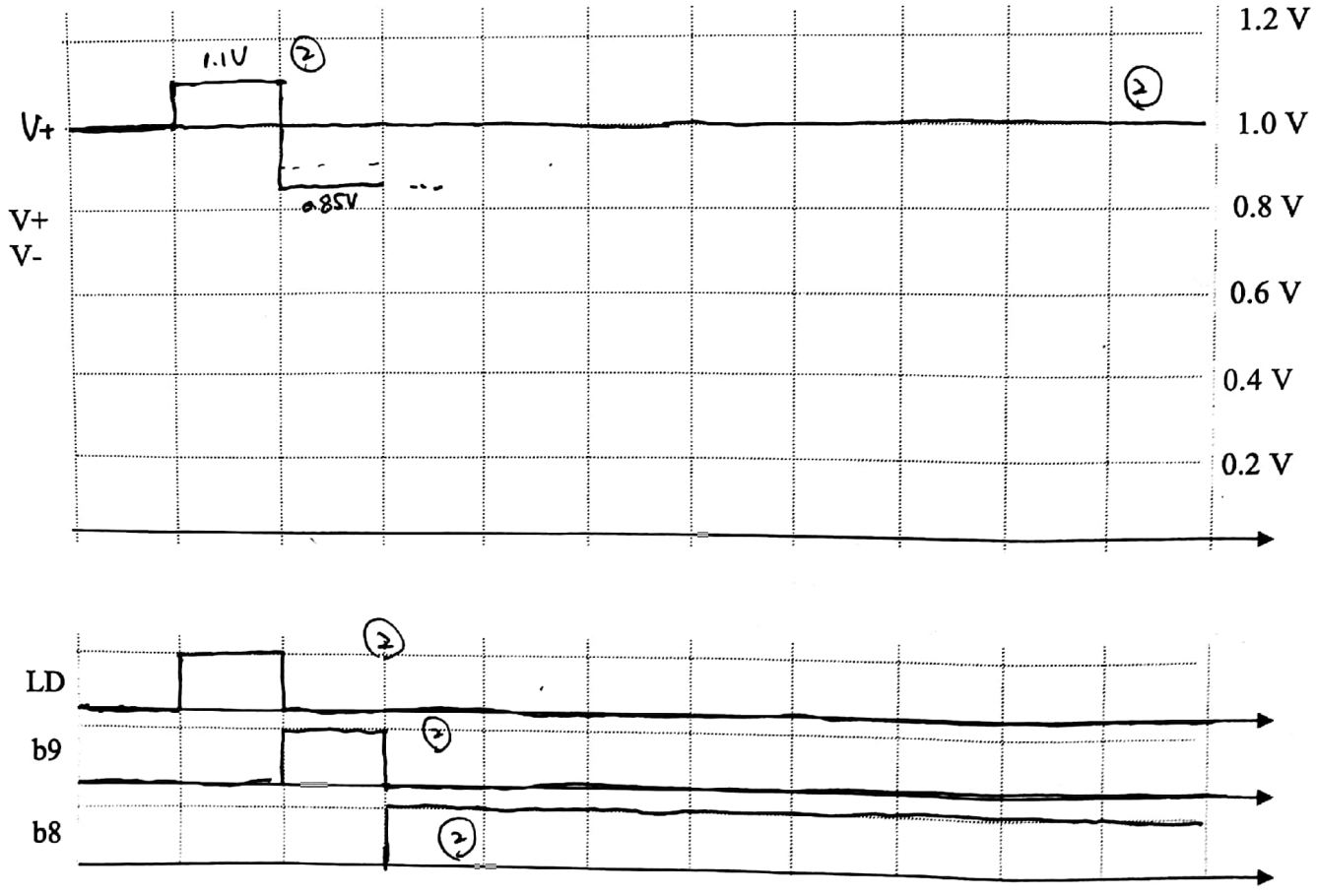
a. [10] draw a schematic of the ADC using an op-amp symbol for the comparator, and transistors and capacitors. Don't draw anything for bits 1 through 8, but do draw bits 0 and 9. Assume that there is a 10 bit digital SAR controller supplied to you.



b. [2] if the unit capacitance is 2 fF, what is the total input capacitance of the ADC?

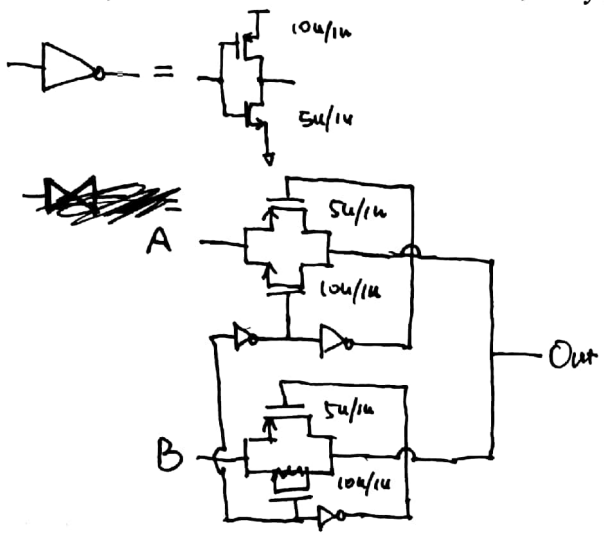
$C = 2^{10} \cdot 2 = 2^{11} = 2048fF$

c. [10] sketch the waveforms for the first two bit decisions (b9 and b8) for an input of 0.4V. Specifically, sketch LD, b9 and b8 on the lower axes, and both V+ and V- of the comparator on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.



2-input MUX. Inputs will be between 0 and 1V (not 0 and V_{DDA})

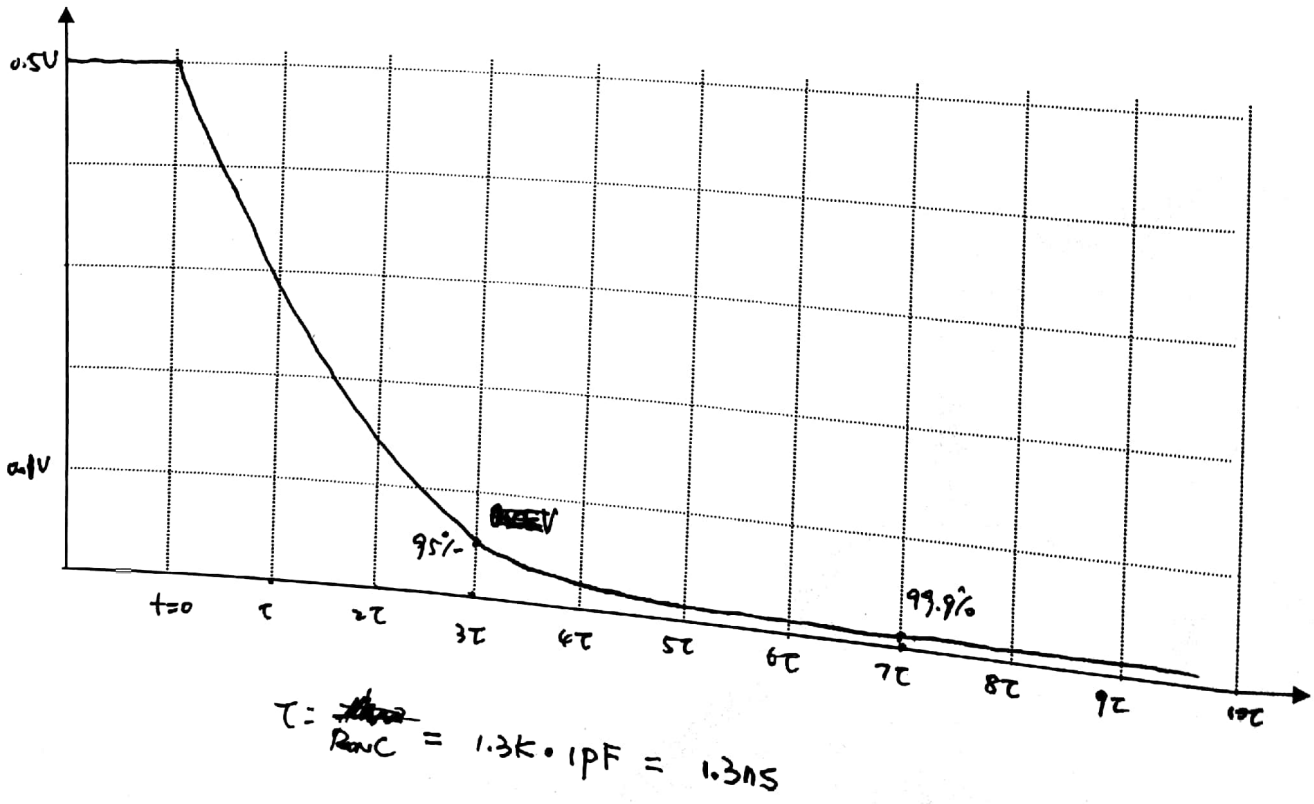
a. [4] draw the schematic of the transistor implementation. Label W/L values. Assume that the control bit is in the analog power domain (0, VDDA). If you need a digital logic cell, draw the transistors schematic.



b. [2] estimate the MUX "on" resistance for an input near 0V (I want an answer in Ohms, not a formula)

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{DDA}-V_{TH})} = \frac{1}{200\mu \times 5 \times 0.75V} = \frac{4}{3}k \approx 1.3k\Omega$$

c. [4] The MUX, with one input at 0V and one input at 0.5V, is driving a 1pF capacitor. Carefully sketch the voltage waveform when the input to the MUX select switches from the 0.5V input to the 0V input. Label the axes. Label the times when the settling accuracy is at 95%, and 99.9%



$\tau = R_{on}C = 1.3k \cdot 1pF = 1.3ns$