1. [8] The I-V curves below are from an Indium Gallium Zinc Oxide transistor used in flat panel display TVs.

   a. Estimate $g_m$ when $V_{GS}=10\text{V}$ and $V_{DS}=10\text{V}$. Write down what $\Delta I$ and $\Delta V$ you are using for your calculation.

   

   $$g_m \approx \frac{\Delta I}{\Delta V}, \text{ for } \Delta V = 2.5\text{V},$$

   

   $$\frac{0.01}{2.5} \approx 0.004 \text{mA/V}$$

   

   b. Estimate $g_n=1/r_n$ under the same conditions. Draw the line that you are using to estimate $g_n$. say slope $x = \frac{0.01}{10\text{V}}$, $0.001 > g_n$

   

   c. Calculate the intrinsic gain from parts a and b

   

   $$\frac{0.01}{2.5} = \frac{0.01}{0.004} = \frac{25}{4}$$

   

   d. If $I_{DS}=10\text{nA}$ when $V_{GS}=2\text{V}$, estimate the sub-threshold slope.

   

   

   

   $$V_{GS} > -3 \text{ on a log} \nu \text{ scale}$$

   

   So, $g_{decades}/\Delta V \approx 10$

---

(Li et al., "High-speed dual-gate a-IGZO TFT-based circuits ...", 2014)
2. [10] For the current mirror shown here,

a. Draw the small signal model of the circuit, assuming that the amplifier is an ideal op-amp with a large positive gain $A$, and that $V_{\text{ref}}$ is a constant voltage.

![Small signal model of the current mirror](image)

b. What is the minimum value of $V_{\text{ref}}$ for which transistor M1 will remain in saturation? If we compare this circuit to a typical simple current mirror, which has a lower minimum input voltage? Why?

$V_{\text{ref}} > V_{\text{out}}$, which is lower than the simple mirror.

c. Write an expression for the small-signal input impedance of the current mirror. How does that compare to a simple current mirror?

$$R_i \approx \frac{1}{g_{m}A}$$

2. Write an expression for the output impedance of the current mirror

$$R_o = \frac{1}{g_{m}}$$

3. [10] You are designing a single-stage CMOS op-amp to be used in feedback to achieve a gain of 5. The gain must be accurate to 1% from DC to 1 Mrad/s (including any 3dB losses). The load is a 10 pF capacitor. You are restricted to biasing your transistors with overdrives between 100 mV and 1 V, and they look reasonably quadratic in that range. $f = 1/5$

4. a. What is the minimum open-loop gain and dominant pole location of the op-amp?

$$A_{\text{pk}} = 0.01$$

b. What is the minimum unity gain frequency of the op-amp?

$$f_u = \frac{1}{2\pi R C} = \frac{1}{2\pi \times 10 \text{ M} \text{Hz}}$$

c. What is the minimum transconductance of the input transistors?

$$g_m = \frac{V_u}{I_u} = \frac{5 \times 10^{-8}}{500 \text{ mV} / \text{V}} = 10^{-3}$$

d. What is the minimum current in each of the input transistors?

$$I_D = \frac{5 \times 10^{-8}}{2} = 2.5 \times 10^{-8} \text{ mA}$$
[16] For the figure below you may assume that the switches and op-amp are ideal. \( \phi_1 \) and \( \phi_2 \) are non-overlapping clocks. Assume all of your capacitors are initially discharged.

a. After the first round of \( \phi_1 \) and \( \phi_2 \) (we'll call it cycle 0), what is the charge, \( Q_F[0] \), on the right side of \( C_F \) in terms of that cycle's input, \( V_{IN}[0] \)?

\[
Q_S[0] = Q_X[0] = C_S(0-V_{IN}[0]) = C_F(0-V_{OUT}[0]) = -Q_F[0]
\]

\[ Q_F[0] = C_S V_{IN}[0] \]

b. What is the corresponding voltage, \( V_{OUT}[0] \)?

\[
V_{OUT}[0] = \frac{C_S}{C_F} V_{IN}[0] = \frac{Q_F[0]}{C_F}
\]

c. Now the input voltage has changed to \( V_{IN}[1] \). What is the charge \( Q_F[1] \) on the right side of \( C_F \) after the next cycle in terms of \( Q_F[0] \) and \( V_{IN}[1] \)?

\[
Q_S[1] = Q_C(-V_{IN}[1]) \Rightarrow Q_F[1] = Q_F[0] + Q_S[1]
\]

\[ Q_F[1] = Q_F[0] + C_S V_{IN}[1] \]

d. Write an expression for \( V_{OUT}[n] \), the output voltage after \( n \) cycles.

\[
V_{OUT}[n] = \frac{Q_F[n]}{C_F} = \frac{C_S}{C_F} \sum_{i=0}^{n} V_{IN}[i]
\]

e. What do we call this kind of circuit?

integrator

Same circuit, different types of questions:

f. During \( \phi_2 \) what is the feedback factor for the amplifier?

\[
f = \frac{C_F}{C_S + C_F}
\]

g. During \( \phi_2 \) what is the total capacitance at the output of the amplifier?

\[
C_{out(2)} = C_L + (1-f) C_F
\]

h. If there is parasitic capacitance \( C_P \) on node \( V_- \), does that change the feedback factor during \( \phi_2 \), and if so, what is the new feedback factor?

\[
f = \frac{C_F}{C_F + C_L + C_P}
\]
[15] Given the cascode amplifier below, $g_m=1$ms and $r_o=10k$. $C_L=2pF$, $C_{gs}=100pF$ and you may assume that all other capacitors are zero. The current source has an output impedance of $1M$.

On the next page, plot the magnitude of the output impedance, $Z_{out}$, vs. frequency. LABEL AXES CLEARLY $Z_0 = r_{in}^2 \parallel 1M = 10^{-3} \cdot 10^8 \parallel 1M \approx 10^5$.

b. What is the output pole frequency?

$$P_2 = \frac{1}{10^5 \cdot 10^{-12}} = \frac{1}{5 \cdot 10^{-7}} = 5M \text{ rad/s}$$

c. What is the low frequency impedance seen looking into the source of M2?

$$\left| \frac{1}{g_{m1} \left( R_o \ || \ Z_{s2} \right)} \right| \approx 10^4 \cdot 10^3 = 10^7 \Omega$$

d. What is the low frequency gain from $V_{in}$ to the drain of M1?

$$\left| \frac{g_{m1}}{g_{m2} \left( R_o \ || \ Z_{s2} \right)} \right| \approx 10^4 \cdot 10^3 = 10^7 \Omega$$

e. What is the low frequency input capacitance if $C_{gd}=20pF$?

Miller Cap! $C_{gd} \ (1+10) = 220pF$. Add $C_{gs}$ for $C_{in}$

$$C_{in} = 220pF + 100pF = 320pF$$

f. Plot the magnitude of the impedance looking into the source of M2, $Z_{s2}$, vs. frequency. LABEL AXES CLEARLY $Z_{s2} = \frac{1}{g_{m2} \left( 1+ \frac{1}{g_{m2} \left( 1+ \frac{1}{g_{m2} \left( 1+ R_o \ || \ Z_{s2} \right)} \right)} \right)}$.

What is the second pole frequency? What’s the dominant pole? Note $Z_2$ will roll-off when $\frac{1}{s \ C_{CL}} = 1M \ \Omega \ \text{or } s = 5 \times 10^5 \text{ rad/s}$. At this frequency $\frac{1}{s \ C_{CL}}$ is still very large, & so is inconsequential. Magnitude of $Z_{out}$ so when $Z_2(s) \approx 1$, $Z_{out}(s) \approx 10^5$.

Z2 is still $\frac{1}{g_{m2} \left( 1+ \frac{1}{g_{m2} \left( 1+ \frac{1}{g_{m2} \left( 1+ R_o \ || \ Z_{s2} \right)} \right)} \right)}$.

Magnitude of $Z_{out}$ is when $\frac{1}{s \ C_{CL}} = 10^5 \ \text{rad/s}$.

- Zero @ $1 = \frac{R_o(s)}{R_o} \ \text{or when } Z_2(s) = r_o$
- This is when $\frac{1}{s \ C_{CL}} = 10^4 \ \text{& } s = 5 \times 10^7 \ \text{rad/s}$.

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Scanned by CamScanner
For the figure below, $V_{tn} = -V_{tp} = 1V$. The overdrive voltage on M5 and M7 is 100 mV. You may ignore body effect, and assume that the devices all look quadratic.

a. Assuming $\lambda = 0$, estimate the currents in on the transistors in the table below.

The square root of 20 is approximately 4.5

| $|I_D|$ | M1   | M3   | M5   | M7   | M9   | M11  | M16  | M17  |
|------|------|------|------|------|------|------|------|------|
| 0 a  | 200 uA | 200 uA |
| 3V   | 3.9V | 3.9V | 1.1V | 1.1V | 1.45V | 3.9V | 3.55V |

b. Assuming $\lambda = 0$, estimate the bias voltages on the gates of the transistors in the table below.

c. Estimate the input common mode range (give a voltage for each)

$$V_{icm, \text{min}} = 0 \text{ V}$$
$$V_{icm, \text{max}} = 3.8 \text{ V}$$

d. Estimate the output swing for which all transistors will remain in saturation

$$V_{o, \text{min}} = 0.45 \text{ V}$$
$$V_{o, \text{max}} = 4.55 \text{ V}$$

5V VDD 200 uA

20x smaller $\rightarrow$ 5x larger

$5V - 4.5V = 3.55V$
For the following problems related to the project, you will be working in a CMOS process with 
\[ \mu_n C_{ox} = 200 \mu A/V^2, \mu_p C_{ox} = 100 \mu A/V^2, \quad V_{tn} = -V_{tp} = 0.5V \text{ and } \lambda = 1/(10V) \text{ (1um/L)} \text{ with } W_{min}=l_{min}=1\text{um}. \] Note that this is NOT the same process as you used for your project this semester.

The supply is 2 alkaline cells, so \( V_{bat} = 1.6..3.2V \)

You will design parts of the following analog blocks

- A low voltage bandgap reference
- an analog regulator with an output of 1.25 V
- an ADC reference voltage of 1V
- a digital regulator with an output of 1.5 V
- a 2-input analog multiplexer with a single control bit
- a programmable gain amplifier with one gain select bit, and a gain of either 1 or 5
- a 10 bit switched capacitor ADC. **The ADC has an input range from 0-1V.** This is less than \( V_{DDA} \).

op-amp topologies for parts “b” below: N or P input; 5 transistor, current mirror, 2 stage, folded cascode

7. [8] To get started, carefully sketch the drain current vs. drain voltage for an NMOS transistor with 
\( W/L=10u/1u, V_{GS}=0.7V \), from \( V_{DS}=0 \) to \( 1V \). Label the axes. Label the transition from triode to saturation.

\[
\begin{align*}
I_{ds} &= \frac{1}{2} \mu C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \\
V_{T} &= 0.7V \
V_{GS} &= 0.4V \
V_{DS} &= 0.2V \
V_{DS} &= 1.0V
\end{align*}
\]

\[
\begin{align*}
\Rightarrow V_{DS} &= 0.2V: \quad \frac{1}{2} \frac{(200 \ \mu A/V^2)}{V^2} (0.2)^2 (1 + 0.02) \
&= 100 (0.04) (10)(1.02) = 40 (1.02) \\
V_{DS} &= 1.0V: \quad \frac{1}{2} (200)(10)(0.04)(1.1) = 40.08 (10) \\
&= 40.8 \mu A
\end{align*}
\]
For the above circuit, assume that the op-amp is high gain and the transistors are identical with high output impedance.

2 a) Explain why (prove) the three currents labeled "I_1+I_2" must be equal, why the two currents labeled I_2 must be equal, and why the two currents labeled I_1 must be equal.

\[ V_1 = V_2 \quad \text{and} \quad I_2 = V/R_2 \quad \text{for both sides} \]

\[ I_1 = I_2 \quad \text{equal both sides due to mirror M1 & M2} \]

\[ I_1 = \text{equal both sides due to above (algebra)} \]

2 b) What is the voltage across R_2?

\[ V_{\text{thermal}} = \ln(N) \cdot V_{\text{thermal}} \]

2 c) Write expressions for I_1 and I_2 in terms of V_{eb2} (the right diode voltage), V_thermal (thermal voltage), R_1, N, and R_2.

\[ I_1 = \frac{V_{eb2}}{R_1}, \quad \text{PTAT} \]

\[ I_2 = \frac{V_{eb2}}{R_2}, \quad \text{CTAT} \]

2 d) For I_1 and I_2, which one is PTAT, which one has a negative temperature coefficient?

\[ I_1 \quad \text{PTAT} \quad I_2 \quad \text{CTAT} \]

2 e) Put it all together: Find the equation for V_{ref}!

\[ V_{\text{ref}} = (I_1 + I_2) R_3 = \frac{R_3}{R_2} \left( V_{eb2} + \frac{R_2}{R_1} \ln N \cdot V_{\text{thermal}} \right) \]

2 f) Roughly what should the ratio between R_1 and R_2 be to get zero temperature coefficient on V_{ref}? Write one as an integer times the other.

\[ R_1 = \frac{3000 \text{mV/k}}{0.085 \text{mV/k} \cdot \ln(N)} \]

2 g) Roughly what should the ratio between R_2 and R_3 be to get V_{ref} = 0.6 V? Write one as an integer times the other.

\[ R_3 = \frac{1}{2} R_2 \quad \text{or} \quad \frac{R_3}{R_1} = \frac{1}{2} \]

1 b) Give the minimum required supply voltage for this circuit if the mirror transistors have a V_{ow} of 200mV and V_{eb2} = 0.65V.
Regulators. You decide not to use the fancy low-voltage bandgap, and go back to a traditional one.

4. [9] draw the schematic for the analog regulator (1.25V), digital regulator (1.5V), and ADC reference regulator (1V) using op-amp symbols, assuming that the bandgap is producing \( V_{BG} = 1.25V \). If you use resistors, clearly indicate what their ratios should be.

![Analog Schematic](image1)

![Digital Schematic](image2)

ADC reference:

\[
\frac{R_2}{R_1 + R_2} = 1.25
\]

\( R_1 = R_2 = 1.25 \)

\( R_1 = 1k\Omega, \ R_2 = 5k\Omega \)

b. [5] for the digital regulator op-amp:

i. what is the common mode input?

\( 1.25V \)

ii. what is the output swing needed?

\( V_{0O} - V_{th} - V_{op} \approx V_{dd} - V_{th} \)

iii. what is the voltage supply?

\( 1.6V - 3.2V \)

iv. which topologies will NOT work, and why?

- Prods input will not work
Gain of 1 or 5 PGA

a. [10] draw the schematic using an op-amp symbol, transistors, and capacitors. Assume that the gain control bit G and two non-overlapping clock phases \( \phi_1 \) and \( \phi_2 \) are in the analog power domain \((0, V_{DDA})\). If you need a digital gate, draw the schematic using transistors.

b. [5] for the op-amp:
   i. what is the common mode input? 
      \( 0 \) V
   ii. what is the output swing needed? 
      \( 0 - V_{DGA} \) or \( 0 - V_{DQ} \)
   iii. what is the voltage supply 
      \( V_{OOD} \)
   iv. which topologies will NOT work, and why?
      1) NMS input not work
      2) ST
      3) without a output stages
ADC. Vin=0 to 1V. The reference voltage is 1V. The analog supply is 1.25 V.
a. [10] draw a schematic of the ADC using an op-amp symbol for the comparator, and transistors and capacitors. Don't draw anything for bits 1 through 8, but do draw bits 0 and 9. Assume that there is a 10 bit digital SAR controller supplied to you.

b. [2] if the unit capacitance is 2 fF, what is the total input capacitance of the ADC?

\[ C = 2^0 \cdot 2 = 2 = 2 \text{fF} \]

c. [10] sketch the waveforms for the first two bit decisions (b9 and b8) for an input of 0.4V. Specifically, sketch LD, b9 and b8 on the lower axes, and both V+ and V- of the comparator on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.
2-input MUX. Inputs will be between 0 and 1V (not 0 and \(V_{DDA}\)).

a. [4] draw the schematic of the transistor implementation. Label W/L values. Assume that the control bit is in the analog power domain (0, \(V_{DDA}\)). If you need a digital logic cell, draw the transistors schematic.

b. [2] estimate the MUX "on" resistance for an input near 0V (I want an answer in Ohms, not a formula)

\[
R_{on} = \frac{1}{\mu C_{on} \frac{W}{L} (V_{DDA} - V_{IN})} = \frac{1}{2 \mu A \times 5 \times 0.75V} = \frac{6}{5} \approx 1.2 \Omega
\]

c. [4] The MUX, with one input at 0V and one input at 0.5V, is driving a 1pF capacitor. Carefully sketch the voltage waveform when the input to the MUX select switches from the 0.5V input to the 0V input. Label the axes. Label the times when the settling accuracy is at 95%, and 99.9%.