EE140/240A Midterm 2
2020 Spring

You may spend up to two contiguous hours to take this exam.
The exam is open book, open notes. You may view reference materials stored in a single directory on your computer or phone. All other use of electronics is prohibited.

Name_____

SID_____

Exam start time:_____

Exam end time:_____

I didn't cheat and I won't cheat on this exam _____ (signature)

Problem	Score	Points Possible
1		15
2		12
3,4		13
5,6		20
7		14
8		12
Total		86

1) You have an op-amp with a low-frequency gain of 1,000,000 and a single pole at 1 rad/s.
   a. [3] Carefully sketch the location of the pole in the s-plane as a function of the feedback factor f from f=0 to 1. Label where f=0 and where f=1.

   b. [12] Now with f=0.01
      i. Carefully plot the straight-line approximation of the Bode plot (magnitude and phase) of the closed-loop amplifier. Label ω_p, ω_u, and the important frequencies on the phase plot.

      ii. What is the fractional gain error at low frequency?

      iii. What is the unity gain frequency?

      iv. How does it compare to the open-loop unity gain frequency?

2) [12] For the LT1008 with feedback compensation capacitor C_F=3 pF,

a. what is the feedback factor f which will give a phase margin of 45 degrees?

b. What is the corresponding closed loop gain?

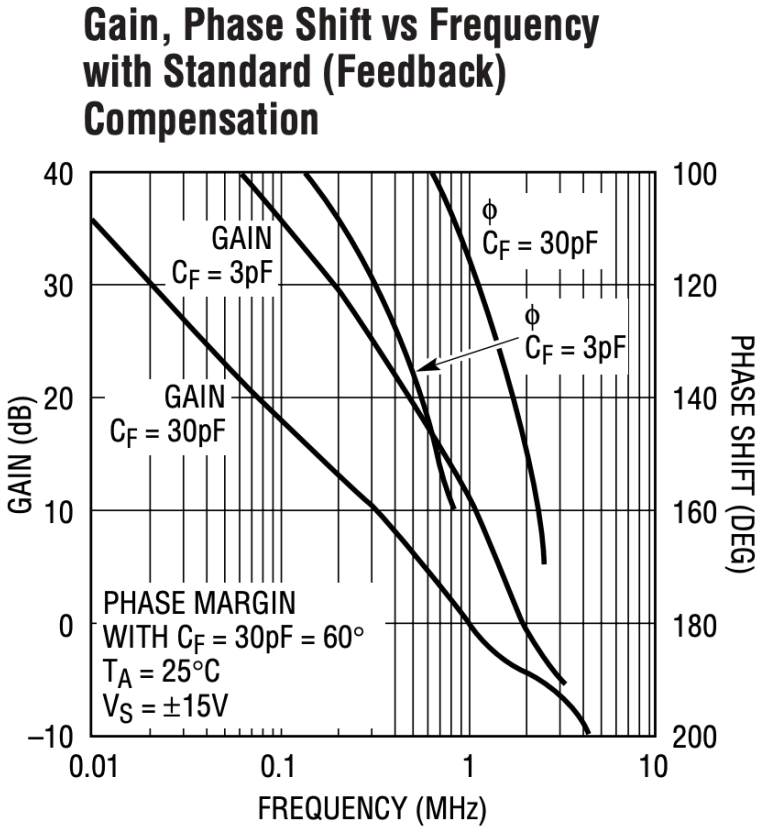
c. If you change f so that the closed loop gain is smaller, will the amplifier be more or less stable?

d. If the amplifier is used with f=0.01, estimate the phase margin of the open-loop system.

e. With C_F=30 pF, is the amplifier unity-gain stable?

f. With C_F=3pF, would you expect that the amplifier is unity-gain stable?

The phase plot below does not continue far enough to answer this question definitively, so to support your answer, draw on the plot below what you are assuming the phase will look like.



3) [5] Slewing
    a. Draw the schematic of an NMOS-input 5T CMOS op-amp.
    b. Redraw the schematic including only those transistors that are on when the op-amp is slewing positive

    c. Draw the schematic of a PMOS-input 5T CMOS op-amp.
    d. Redraw the schematic including only those transistors that are on when the op-amp is slewing positive

4) [8] For a two-stage NMOS-input CMOS op-amp with the output stage biased at **5 mA** and the tail current at **1 mA**
    a. calculate the positive and negative slew rate if $\mathbf{C_c}$**=1pF** and $\mathbf{C_L}$**=1 pF**.

    b. calculate the positive and negative slew rate if $\mathbf{C_c}$**=1pF** and $\mathbf{C_L}$**=10 pF**.

5) [8] For an NMOS-input 5T op-amp with a **5V supply**, $\mathbf{V_{tn}= -V_{tp}=1V}$, and $\mathbf{v_{ov}=0.5V}$ for all devices, sketch the output swing vs. common mode input range. Use clear labels in volts to show the important values at the corners of the plot.

6) A single-pole op-amp has an open-loop gain of 1,000 and a pole at 1 Mrad/s. You may assume that the amplifier is not slewing.

   a. [3] Sketch the response of the amplifier to a 1mV input step on the positive input. Use clear labels on the vertical and horizontal axes, and draw a dotted line for the slope at the origin.

The amplifier is placed into feedback with a feedback factor f=0.1.

   b. [4] What is the low frequency gain and pole location

   c. [2] What is the time constant of the step response

   d. [3] Sketch the response of the closed-loop amplifier to a 1mV input step on the positive input. Use clear labels on the axes, and a dotted line for the slope at the origin.

7) [14] A two-stage CMOS op-amp has a second stage with a gain of 1000 and a pole at 1000 rad/s.

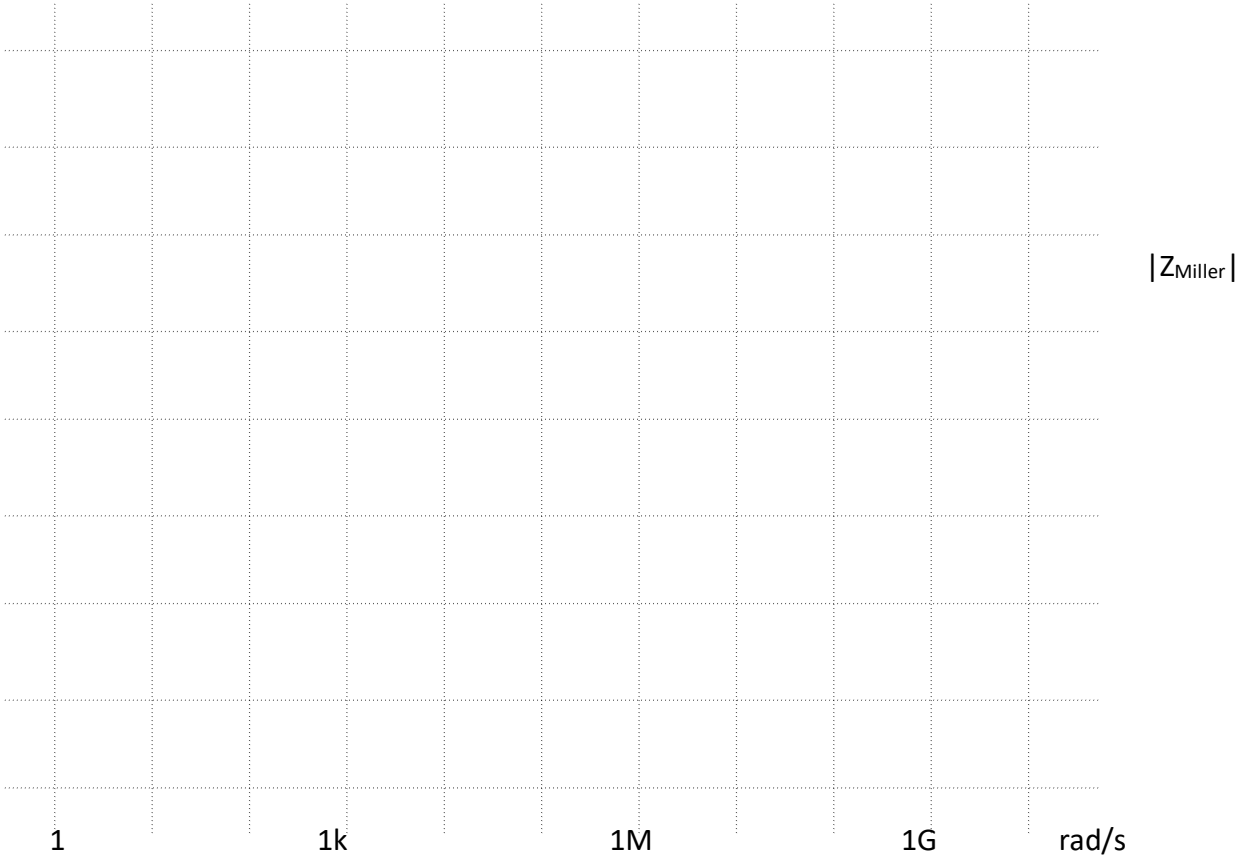
   a. What is the unity gain frequency of the second stage gain?

   b. What is the frequency of the zero in the impedance of the Miller capacitor?

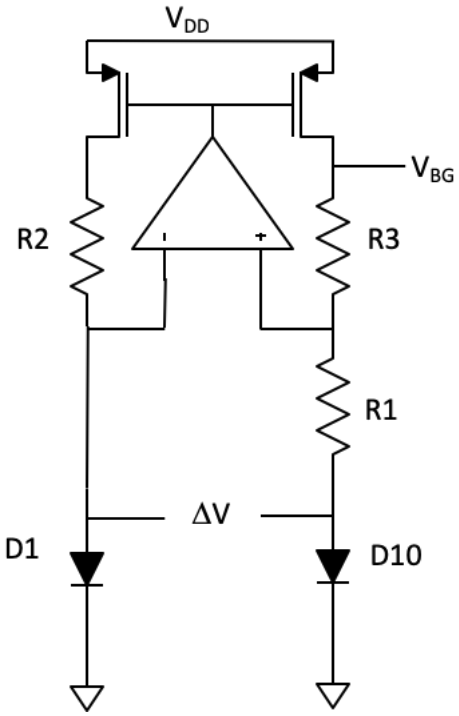
   c. What is the frequency of the pole in the impedance of the Miller capacitor?

With C1=10pF and Cc=1 pF,

   d. Plot the magnitude of the impedance of C1. Label the vertical axis.
   e. On the same plot, plot the magnitude of the impedance seen looking from the first stage in to Cc (i.e. the impedance of the Miller capacitor, Zmiller)



8) [12] The bandgap voltage generator below has diode D1 biased at 0.5V at room temperature and a temperature coefficient of -2.4 mV/K. D10 is ten copies of that diode wired in parallel. Assume that the op-amp is doing its job and the circuit is operating normally.



a. What is the magnitude of the voltage ΔV at room temperature?

b. What is the voltage across R1 at room temperature?

c. On the following page,
   i. plot the voltage on D1 as a function of temperature from 200 to 400 K
   ii. plot the magnitude of ΔV as function of temperature from 200 to 400 K
   iii. Assuming R3=10 R1, plot V_{BG} from 200 to 400K

d. What value of R3 would give the least variation in the bandgap output voltage?


1.2V
1.1V
1V
900mV
800mV
700mV
600mV
500mV
400mV
300mV
200mV
100mV
0 K
300 K
Temperature