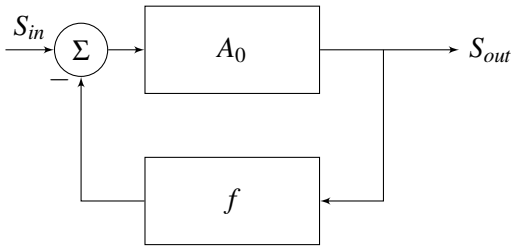
EE 140/240A Linear Integrated Circuits
Spring 2020 Final

1. Feed This Way and That (5 Points)

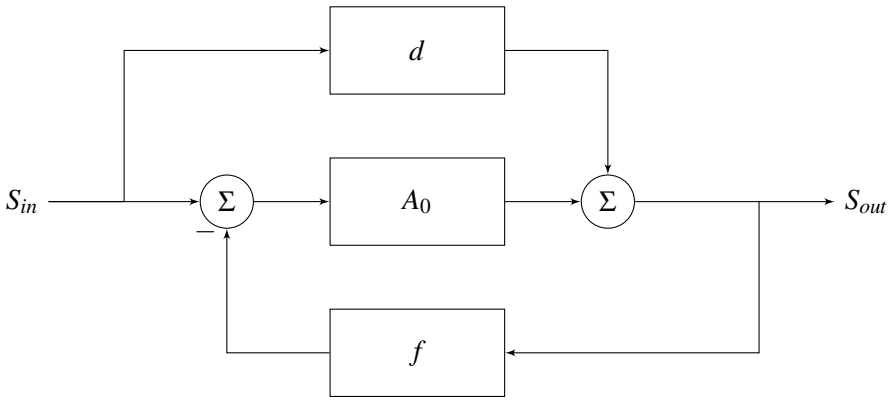


(a) For the system above, find $\frac{S_{out}}{S_{in}}$

Solution: This is a classic feedback-only system (i.e. no feed-forward).

$$\begin{aligned} S_{out} &= A_0(S_{in} - fS_{out}) \\ S_{out}(1+A_0f) &= A_0S_{in} \\ \frac{S_{out}}{S_{in}} &= \frac{A_0}{1+A_0f} \end{aligned}$$

$$\boxed{\frac{S_{out}}{S_{in}} = \frac{A_0}{1+A_0f}}$$



(b) For the system above, find $\frac{S_{out}}{S_{in}}$

Solution: We've now introduced what we call *feed-forward*.

$$\begin{aligned} S_{out} &= dS_{in} + A_0(S_{in} - fS_{out}) \\ S_{out}(1+A_0f) &= S_{in}(d+A_0) \\ \frac{S_{out}}{S_{in}} &= \frac{A_0+d}{1+A_0f} \end{aligned}$$

$$\frac{S_{out}}{S_{in}} = \frac{A_0 + d}{1 + A_0 f}$$

2. 3-Terminal Tater (6 Points)

You are given a device with the following equation for its output current:

$$I_{out} = \frac{1}{3}\alpha(V_{in})^3 + \frac{1}{2}\beta(V_{out})^2$$

(a) What is the output resistance R_o of the device?

Solution:

$$R_o = \left(\frac{\partial I_{out}}{\partial V_{out}}\right)^{-1} = \frac{1}{\beta V_{out}}$$

$$R_o = \frac{1}{\beta V_{out}}$$

(b) What is the transconductance G_m of the device?

Solution:

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = \alpha V_{in}^2$$

$$G_m = \alpha V_{in}^2$$

(c) What is the intrinsic small-signal voltage gain of the device? Mind your signs!

Solution:

$$A_{v0} = -\frac{\alpha V_{in}^2}{\beta V_{out}}$$

3. Single Pole Amp Table (12 Points)

Fill in the following table without a calculator for a single-pole amplifier

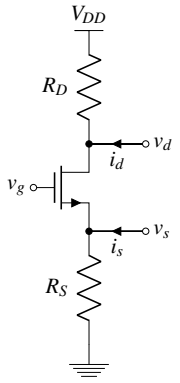
A_{v0} (V/V)	ω_p (rad/s)	ω_u (rad/s)	g_m (1/Ω)	r_o (Ω)	C_L (F)
1000	1M				1p
	1M	0.1G		100k	
		10G		1M	20f
	10	10M			100p

Solution:

$$A_{v0} = |g_m r_o|$$
$$\omega_p = \frac{1}{r_o C_L}$$
$$\omega_u = A_{v0}\omega_p = \frac{g_m}{C_L}$$

A_{v0} (V/V)	ω_p (rad/s)	ω_u (rad/s)	g_m (1/Ω)	r_o (Ω)	C_L (F)
1000	1M	**1G**	**1m**	**1M**	1p
100	1M	0.1G	**1m**	100k	**10p**
200	**50M**	10G	**0.2m**	1M	20f
1M	10	10M	**1m**	**1G**	100p

4. MOSFET Small Signal Transconductances and Impedances (12 Points)



Find the following small signal values for the single-transistor amplifier above. **Your final answers should have the full, unsimplified expression**

(a) $\frac{i_d}{v_g}$ given $v_d = 0\text{V}_{\text{AC}}$. This is the G_m of a degenerated common source.
Solution:

$$\frac{i_d}{v_g} = \frac{g_m r_o}{r_o + R_S + g_m r_o R_s}$$

(b) $\frac{v_d}{i_d}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source-degenerated common source.
Solution:

$$\frac{i_d}{v_d} = R_D || (r_o + R_S + g_m r_o R_S)$$

(c) $\frac{v_d}{v_g}$ assuming $R_D = \infty\Omega$. This is the voltage gain of a degenerated common source amplifier.
Solution: Here you can use the answers from parts (a) and (b). For the latter, because R_D is infinite, $R_o = r_o + R_S + g_m r_o R_S$

$$\frac{v_d}{v_g} = -g_m r_o$$

(d) $\frac{i_s}{v_g}$ given $v_s = 0\text{V}_{\text{AC}}$. This is the G_m of a source follower.
Solution:

$$\frac{i_s}{v_g} = -\frac{g_m r_o}{r_o + R_D}$$

(e) $\frac{v_s}{i_s}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source follower.
Solution:

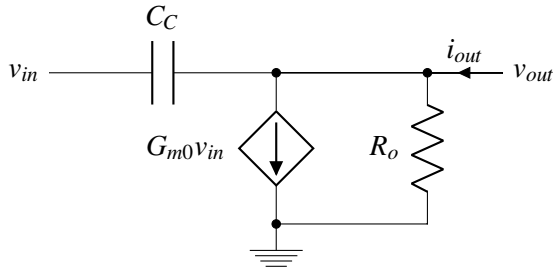
$$\frac{i_s}{v_s} = R_S || \frac{r_o + R_D}{1 + g_m r_o}$$

(f) $\frac{v_s}{v_g}$ assuming $R_S = \infty\Omega$. This is the voltage gain of a source follower.
Solution:

$$\frac{v_s}{v_g} = \frac{g_m r_o}{1 + g_m r_o}$$

5. Compensation Has Consequences (10 Points)

(a) Calculate the $G_m(s)$ of the following circuit:



Solution:

$$\begin{aligned} G_m &= \frac{\partial I_{out}}{V_{in}}|_{v_{out}=0} \\ &= \frac{i_{out}}{v_{in}}|_{v_{out}=0} \end{aligned}$$

Going through KCL

$$\begin{aligned} i_{out} &= G_{m0}v_{in} - sC_C v_{in} \\ &= v_{in}\left(G_{m0} - sC_C\right) \\ \frac{i_{out}}{v_{in}} &= G_{m0} - sC_C \end{aligned}$$

$$\boxed{\frac{i_{out}}{v_{in}} = G_{m0} - sC_C}$$

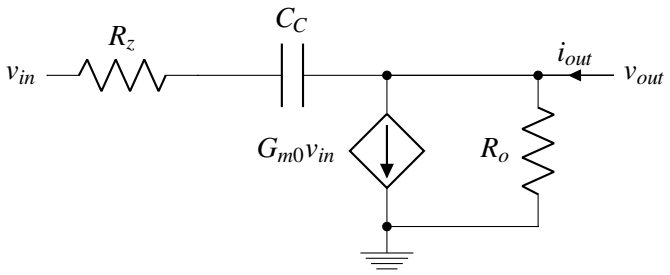
(b) What are the locations of the poles and zeros (if any)? Be sure to specify if they're in the right or left half of the s-plane.

Solution:

$$\begin{aligned} G_{m0} - sC_C &= 0 \\ s &= +\frac{G_{m0}}{C_C} \end{aligned}$$

$$\boxed{\omega_z = \frac{G_{m0}}{C_C} \text{ in the right half plane}}$$

(c) Your colleague proposes the following modification to the previous diagram:



What are the locations of the poles and zeros (if any) of $G_m(s)$? Be sure to specify if they're in the right or left half of the s-plane.

Solution:

Poles

$$1 + sC_C R_z = 0$$

$$s = -\frac{1}{C_C R_z}$$

$$\omega_p = \frac{1}{R_z C_C} \text{ in the left half plane}$$

Zeros

$$G_{m0} + sC_C(G_{m0}R_z - 1) = 0$$

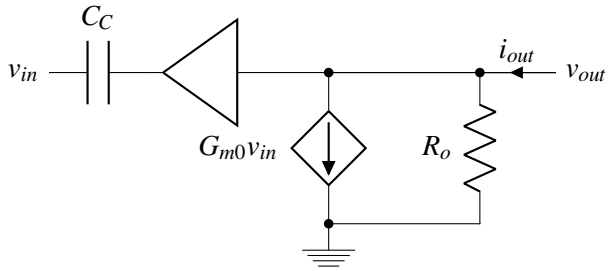
$$s = \frac{G_{m0}}{C_C(1 - G_{m0}R_z)}$$

$$= \frac{1}{C_C\left(\frac{1}{1/G_{m0} - R_z}\right)}$$

$$\omega_p = \frac{1}{R_z C_C} \text{ in the left half plane}$$

$$s_z = \frac{1}{C_C\left(\frac{1}{G_{m0}} - R_z\right)} \text{ where the sign depends on } R_z$$

(d) Calculate the $G_m(s)$ of the following circuit assuming the buffer is ideal (infinite input impedance, zero output impedance):



Solution:

$$i_{out} = G_{m0} v_{in}$$

$$\frac{i_{out}}{v_{in}} = G_{m0}$$

(e) What are the locations of the poles and zeros (if any) of $G_m(s)$? Be sure to specify if they're in the right half or left half of the s-plane.

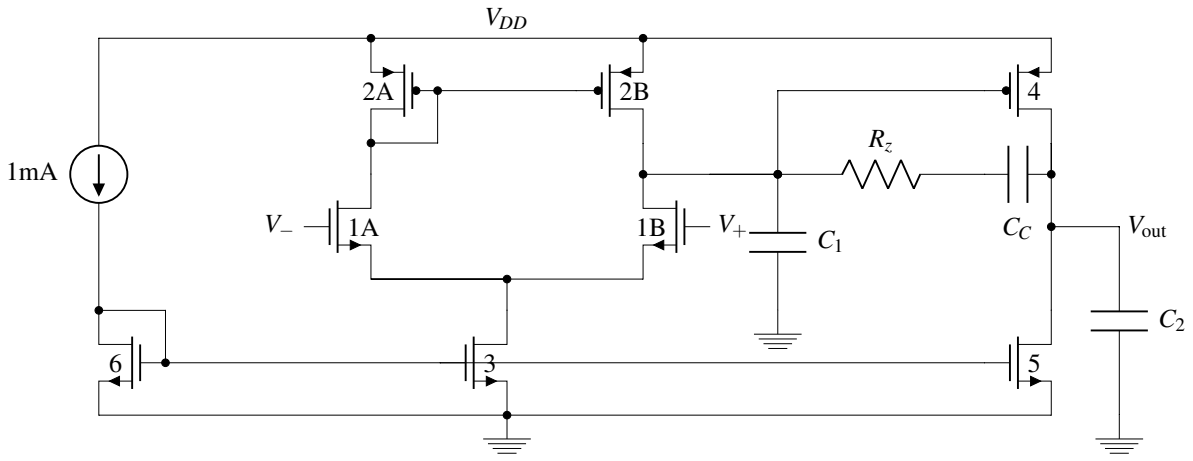
Solution:

> Magic! No poles or zeros in G_m! Practically speaking, the buffer presents some finite load and will have its own frequency response, but the important thing is that the right-half plane zero doesn't appear.

6. Two Stage Drills (24 Points)

Unless otherwise indicated, you may make the following assumptions:

- All transistors are biased in saturation with $V_{ov} = 0.2\text{V}$
- $V_{DD} = 3\text{V}$, $V_{tn} = -V_{tp} = 1\text{V}$
- M3 and M6 are identical. M5 is $5\times$ wider
- All capacitors are assumed to be zero except C_C, C_1, and C_2



(a) What is the common mode input voltage range (min and max)?

Solution:

$$V_{\text{in,min}} = 2V_{ov} + V_{tn} = 1.4\text{V}$$

$$V_{\text{in,max}} = V_{DD} - V_{SG} + V_{tn} = 3 - 1.2 + 1 = 2.8\text{V}$$

$$V_{\text{in}} \in [1.4, 2.8]\text{V}$$

(b) What is the output voltage swing (min and max)?

Solution:

$$V_{\text{out}} \in [V_{ov}, V_{DD} - V_{ov}]$$

$$\boxed{V_{\text{out}} \in [0.2, 2.8]\text{V}}$$

(c) If $C_1 = 0$, $C_2 = 1\text{pF}$, and $C_C = 1\text{pF}$, what is the positive slew rate in $\frac{\text{V}}{\text{s}}$?

Solution: The positive slew rate is determined by the first stage!

$$\begin{aligned}\frac{I_{D3}}{C_C} &= \frac{1\text{mA}}{1\text{pF}} \\ &= 1\frac{\text{V}}{\text{ns}}\end{aligned}$$

$$\boxed{\text{positive slew rate} = 1 \times 10^9 \frac{\text{V}}{\text{s}}}$$

(d) If $C_1 = 0\text{F}$, $C_2 = 10\text{pF}$, and $C_C = 1\text{pF}$, what is the negative slew rate in $\frac{\text{V}}{\text{s}}$?

Solution: We need to consider two things:

First, the first stage with C_C.

$$\begin{aligned}\frac{I_{D3}}{C_C} &= \frac{1\text{mA}}{1\text{pF}} \\ &= 1 \times 10^9 \frac{\text{V}}{\text{s}}\end{aligned}$$

Second, the second stage with C_2

$$\begin{aligned}\frac{I_{D5}}{C_2} &= \frac{5\text{mA}}{10\text{pF}} \\ &= 0.5 \times 10^9 \frac{\text{V}}{\text{s}}\end{aligned}$$

We choose the more restrictive of the two

$$\boxed{\text{negative slew rate} = 0.5 \times 10^9 \frac{\text{V}}{\text{s}}}$$

(e) If $C_1 = 0\text{F}$, $C_2 = 1\text{pF}$, and $C_C = 100\text{pF}$, what is the negative slew rate in $\frac{\text{V}}{\text{s}}$?

Solution: Going through the same process as the previous parts:

First, the first stage with C_C.

$$\begin{aligned}\frac{I_{D3}}{C_C} &= \frac{1\text{mA}}{100\text{pF}} \\ &= 0.01\frac{\text{V}}{\text{ns}}\end{aligned}$$

Second, the second stage with C_2

$$\begin{aligned}\frac{I_{D5}}{C_2} &= \frac{5\text{mA}}{1\text{pF}} \\ &= 5\frac{\text{V}}{\text{ns}}\end{aligned}$$

We choose the more restrictive of the two

$$\text{negative slew rate} = 0.01 \times 10^9 \frac{\text{V}}{\text{s}}$$

A different amplifier with the same topology has the following parameters. You may ignore the pole/zero doublet from the mirror.

$g_{m1,2}$	R_{o1}	g_{m4}	R_{o2}	C_1	C_C	C_2
1mS	10MΩ	1mS	100kΩ	1pF	0.1pF	100pF

(f) If $C_C = 0$F for this part only (magically we will assume no C_{gd4}), what are the uncompensated pole locations?

Solution:

$\omega_{p1,u} = \frac{1}{R_{o1}C_1}$ $\omega_{p2,u} = \frac{1}{R_{o2}C_2}$

$$\omega_{p1,u} = 100\text{krad/s}$$
$$\omega_{p2,u} = 100\text{krad/s}$$

(g) What is the location of the right-half plane zero?

Solution:

$$\omega_{RHPZ} = \frac{g_{m4}}{C_C}$$

$$\omega_{RHPZ} = 10\text{Grad/s}$$

All plots are on the following pages. Don't forget the last parts of the question!

(h) Plot the magnitude of the second stage gain

(i) Plot the overall impedance seen at the first stage output including R_{o1}, C_1, C_C, and any effects of Miller multiplication.

(j) Plot the magnitude of the first stage gain.

(k) Plot the magnitude and phase of the overall gain. **Label any poles and zeros clearly.**

(l) Estimate the unity gain phase margin for this value of C_C.

Solution:

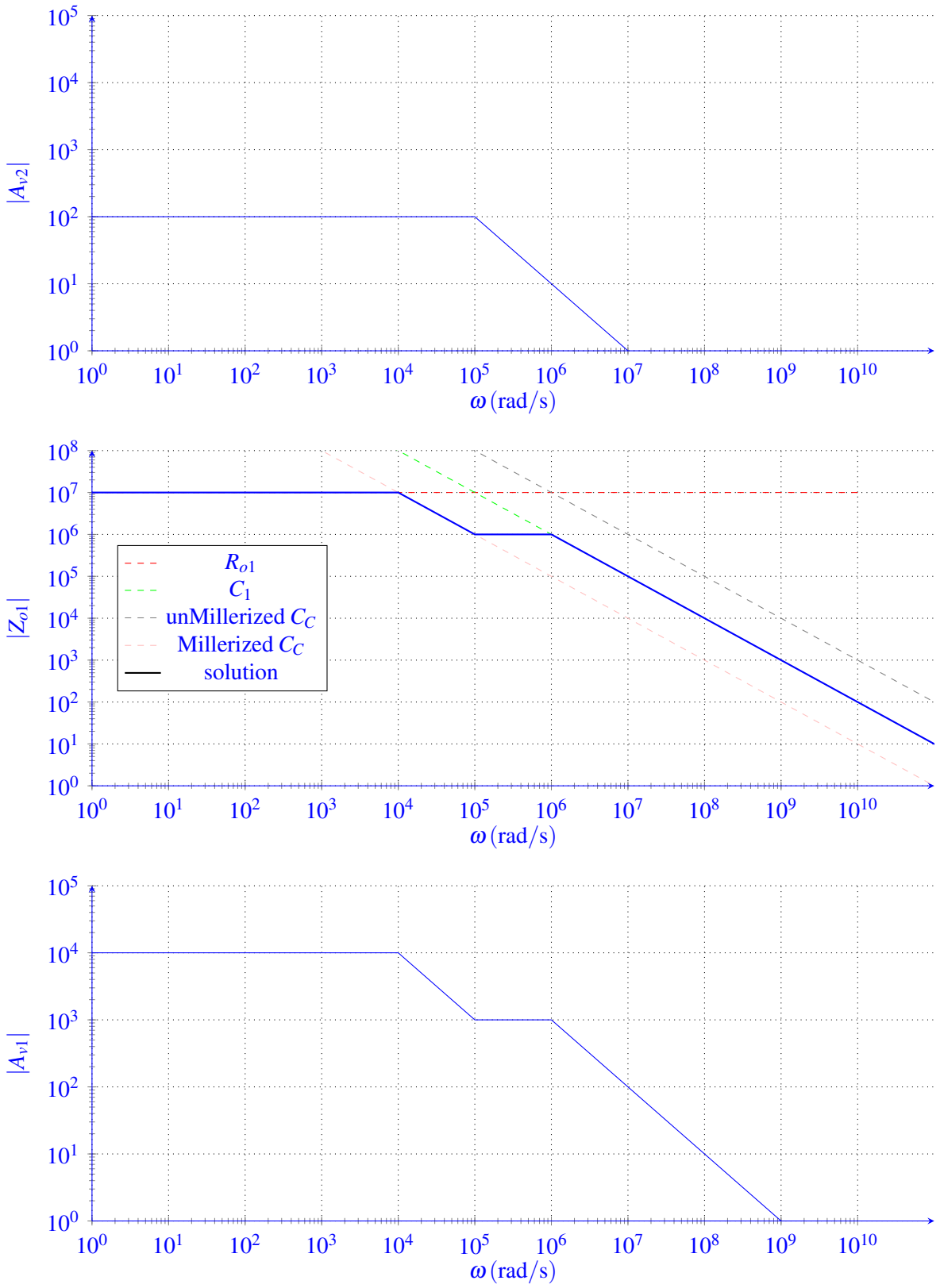
$$0°$$

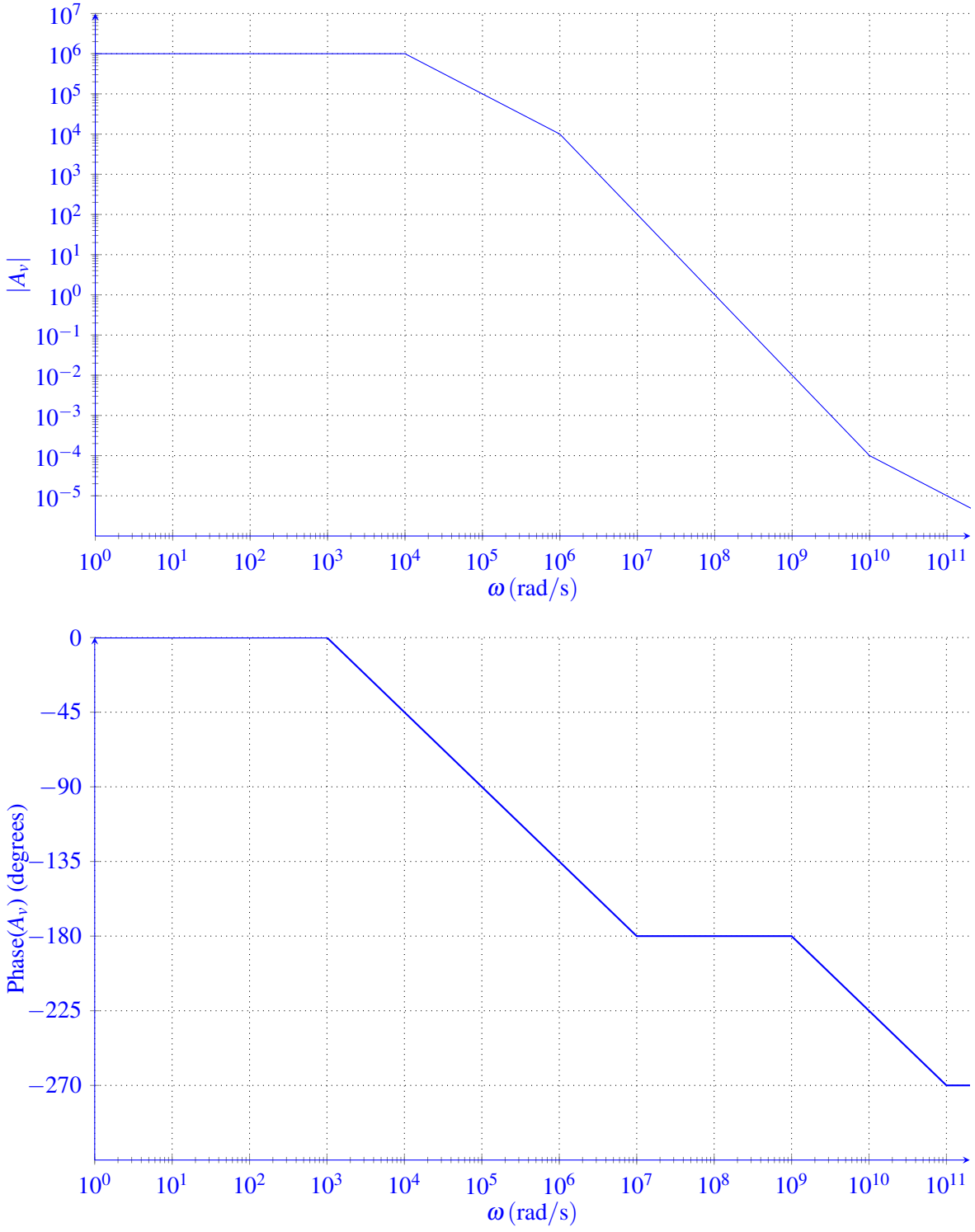
(m) What is the maximum feedback factor and closed-loop gain for which the amplifier has a 45° phase margin?

Solution:

$$f \leq \frac{1}{10^4}$$

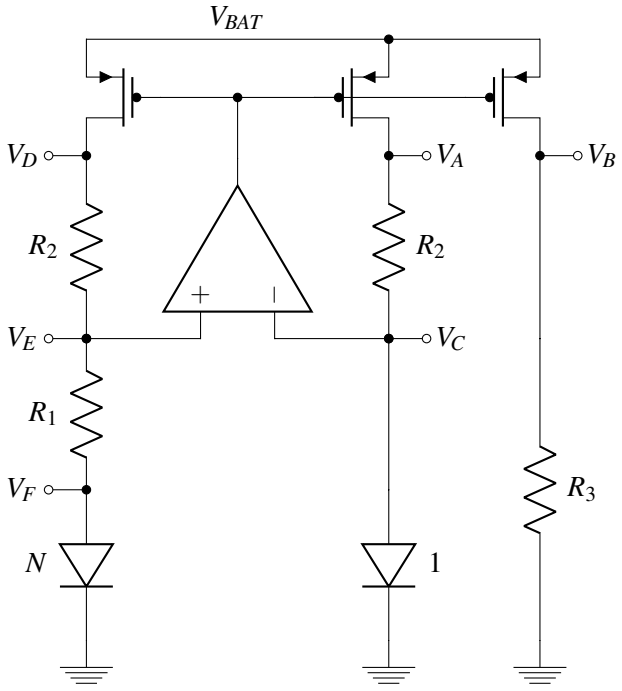
Solution:


$|A_{v2}|$
$|Z_{o1}|$
$|A_{v1}|$
$\omega\,(\mathrm{rad/s})$
R_{o1}
C_1
unMillerized C_C
Millerized C_C
solution



7. Bandgap, Revisited (8 Points)

You're given the following bandgap. You may assume it's functioning exactly as intended, that the amplifier is ideal, and that $\lambda = 0\text{V}^{-1}$ for the MOSFETs.



Indicate if the following are PTAT, CTAT, or independent of temperature.

Solution:

Output	PTAT/CTAT/T-independent?
V_A	T-independent
V_B	PTAT
V_C	CTAT
V_D	T-independent
V_E	CTAT
V_F	CTAT
$V_E - V_C$	T-independent
$V_E - V_F$	PTAT

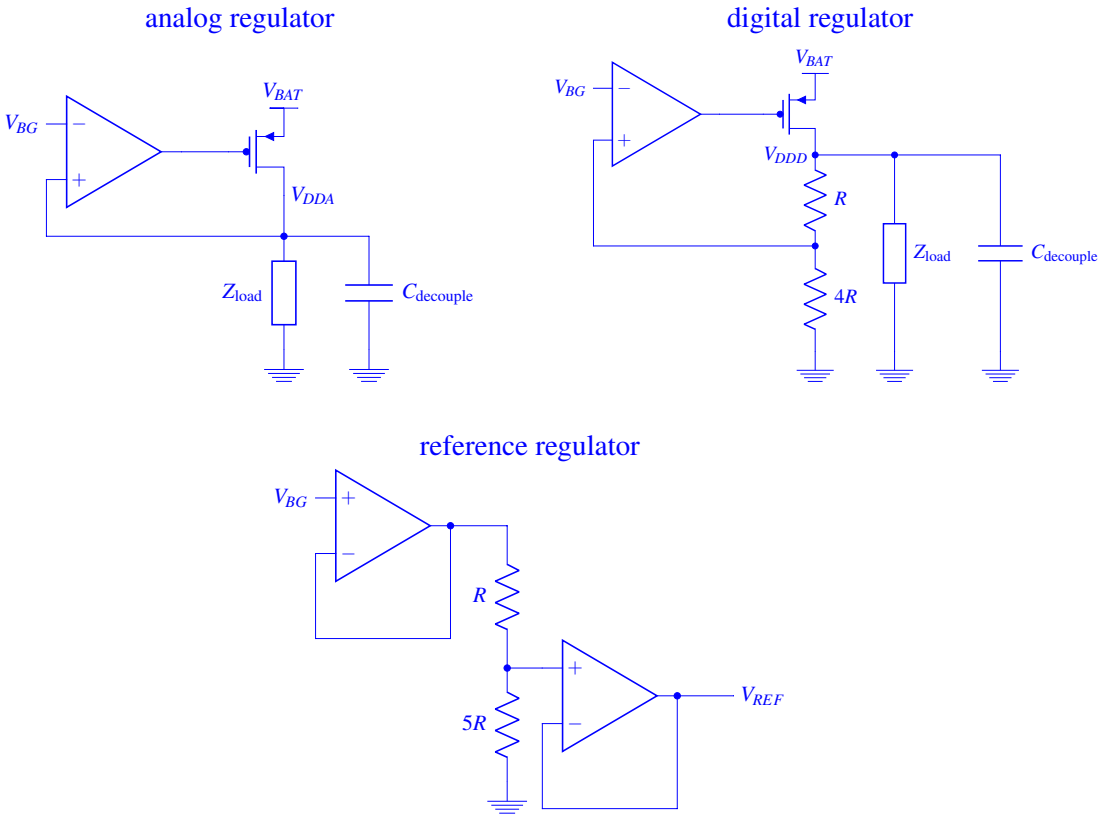
8. Regulate Yoself (14 Points)

(a) You are given a battery $V_{BAT} = 1.6$V, a bandgap reference voltage $V_{BG} = 1.2$V, and devices with

$V_{tn} = |V_{tp}| = 800\text{mV}$. In the box below, draw the schematic for the following. If you use any resistors, clearly indicate their ratios.

i. analog regulator (1.2V)
ii. digital regulator (1.5V)
iii. ADC reference regulator (1V)

Solution:



(b) For the analog regulator op amp

i. What is the common mode input?
Solution:

$$V_{BG} = 1.2\text{V}$$

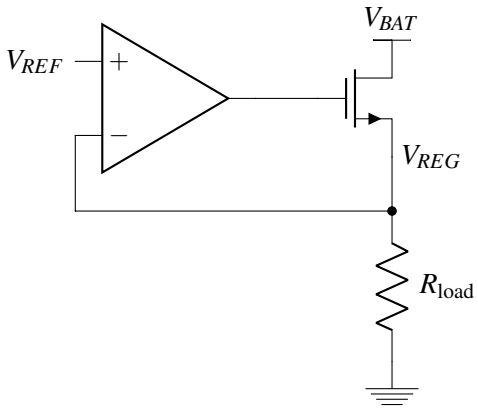
ii. What is the bare necessity for output swing?
Solution:

$$V_{BAT} - |V_{tp}| - V_{ovp} \approx V_{BAT} - |V_{tp}|$$

iii. Which of the following will *not* work? {N/P input}, {5T, current mirror amp, 2-stage common source, folded cascode, 2-stage folded cascode}
Solution:

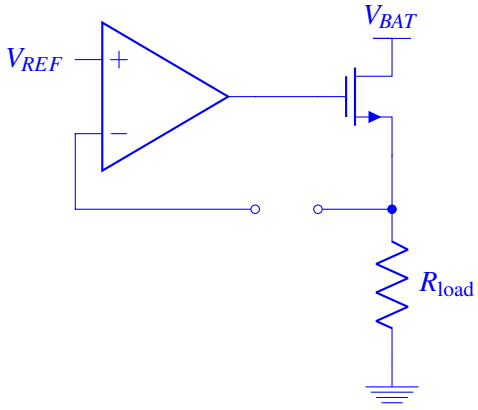
Anything with a PMOS input won't work

(c) Your project partner wants you to verify that the regulator they've made below is stable. The op amp has a differential gain of A_{OL}, and you know the MOSFET's small signal parameters g_m and r_o. Find the magnitude of the loop gain $|T| = A_0 f$ of the regulator.



Solution: To find $A_0 f$ in the feedback diagram, we turn off our input, break every feedback loop (in this case it's just the one) and calculate the gain around the loop one time.

Breaking the loop at the negative input of the amp:



We're interested in a forward pass around the loop, and in this case that means starting on the left side of the break and going around the feedback loop to the other side of the break.

$$\frac{v_r}{v_\ell} = \frac{v_r}{v_g} \cdot \frac{v_g}{v_\ell} \leftarrow g \text{ for gate}$$
$$= -A_{OL} \cdot g_m \left(R_{\text{load}} || \frac{r_o}{1 + g_m r_o} \right)$$

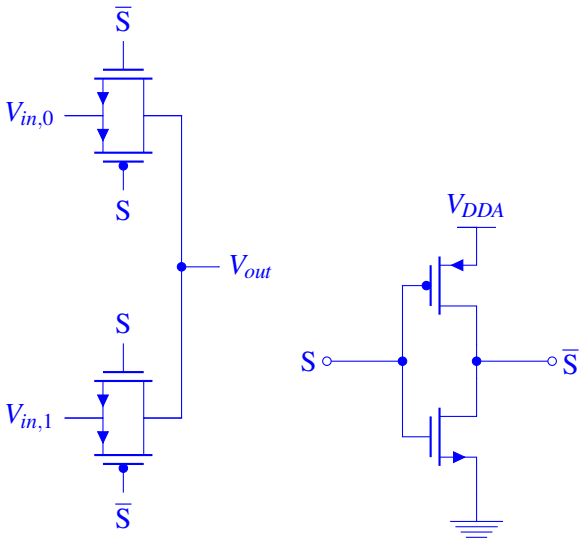
$$|T| = A_{OL} \cdot g_m \left(R_{\text{load}} || \frac{r_o}{1 + g_m r_o} \right)$$

9. 2-Input Mux (8 Points)

For the following 2-input mux, the input voltage can range from 0V to 1V and the control/select bit is in the V_{DDA} power domain (0, 1.2)V.

(a) Draw the schematic of a 2-input mux using transistors. If you need a digital logic cell, draw the transistor schematic.

Solution:



(b) Assuming the following, estimate the mux's on-resistance R_{on} for an input near 0V. **Give a numerical value, not just an equation!**

- Every transistor has $W/L = 1.8\mu m/180nm$
- $V_{tn} = -V_{tp} = 0.4V$
- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu A}{V^2}$

Solution: At low input voltages, the NMOS is on and the PMOS is off.

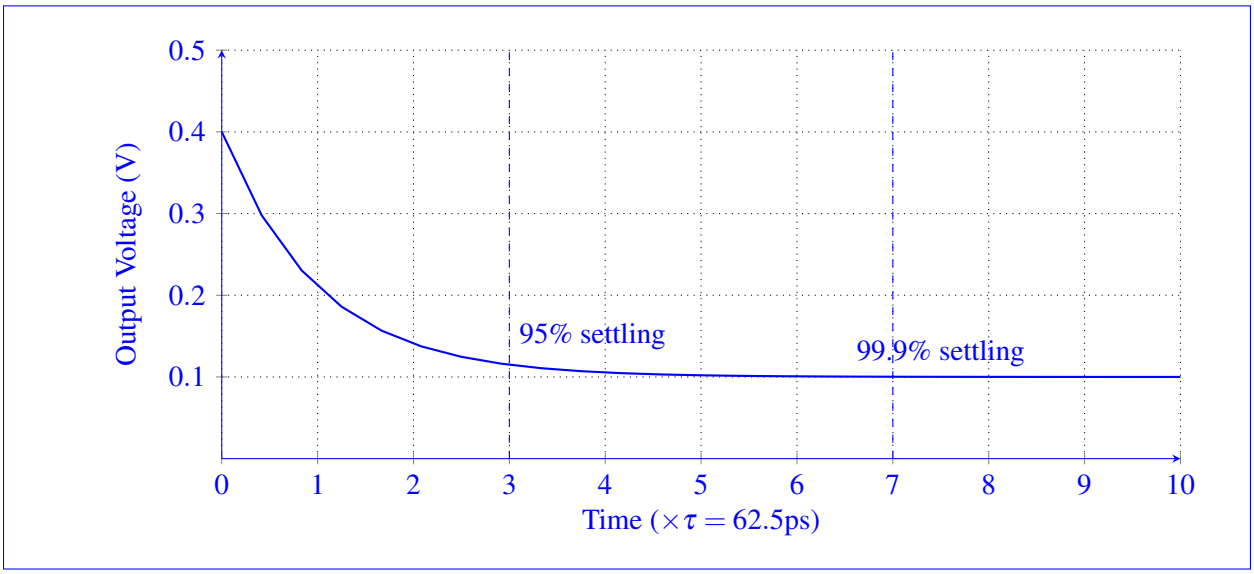
$$\begin{aligned} R_{on} &= \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{DDA} - V_{tn})} \\ &= \frac{1}{16} \times 10^4 \Omega \\ &= 625\Omega \end{aligned}$$

$$R_{on} = 625\Omega$$

Is anything within $\pm 10\%$ acceptable?

(c) The mux is driving a 100fF capacitor and has one input at 0.1V and another at 0.4V. Carefully sketch the voltage waveform when the input to the mux select switches from the 0.4V input to the 0.1V input. Label the axes. Label the times when the settling accuracy is at 95% and 99.9%.

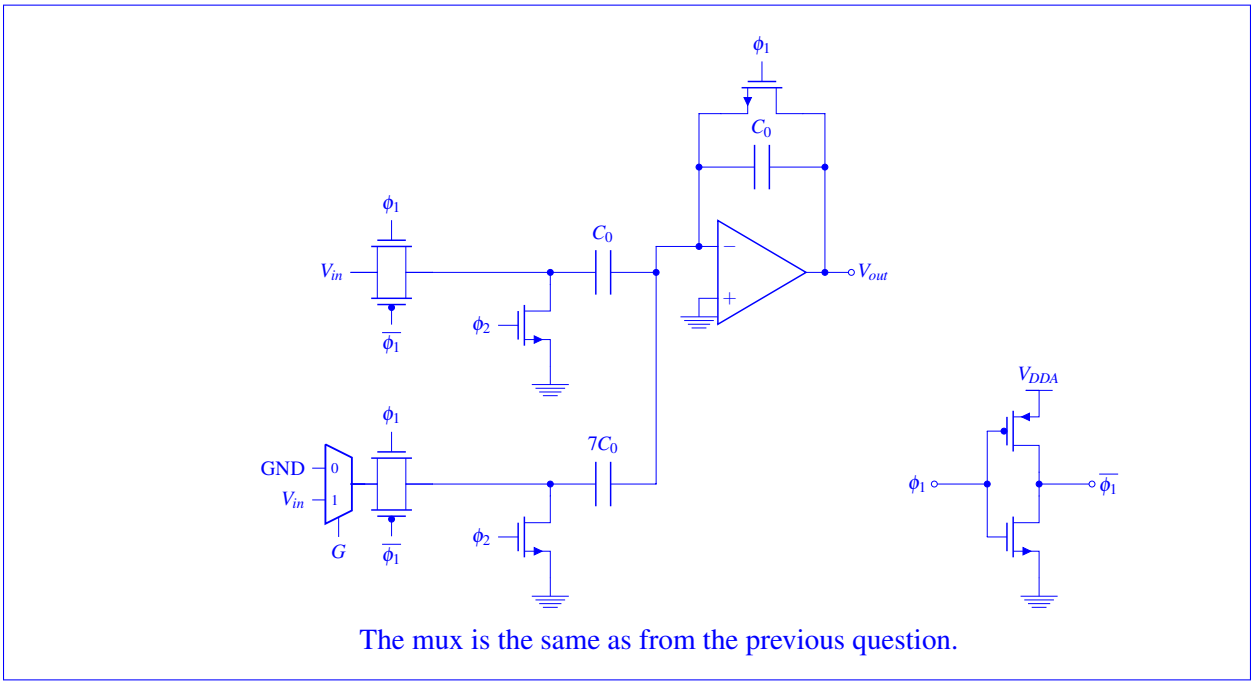
Solution:



10. PGA Gain 1 or 8 (14 Points)

(a) Draw the schematic of a PGA with gain settings of 1 **or** 8. You may use an op-amp symbol, transistors, and capacitors. Assume that the gain control bit G and two non-overlapping clock phases ϕ_1 and ϕ_2 are in the analog power domain (0, V_{DDA}). If you need a digital gate, draw the schematic using transistors.

Solution: Note that this is just one possibility, since the logic can be modified for slightly different switching.



The mux is the same as from the previous question.

(b) For the op amp,

i. What is the common-mode input?

Solution:

0V

ii. If this PGA is feeding into an ADC with a $V_{REF} = 1\text{V}$, what is the output swing needed?
Solution:

0V to 1V

iii. What type of input pair will *not* work?
Solution:

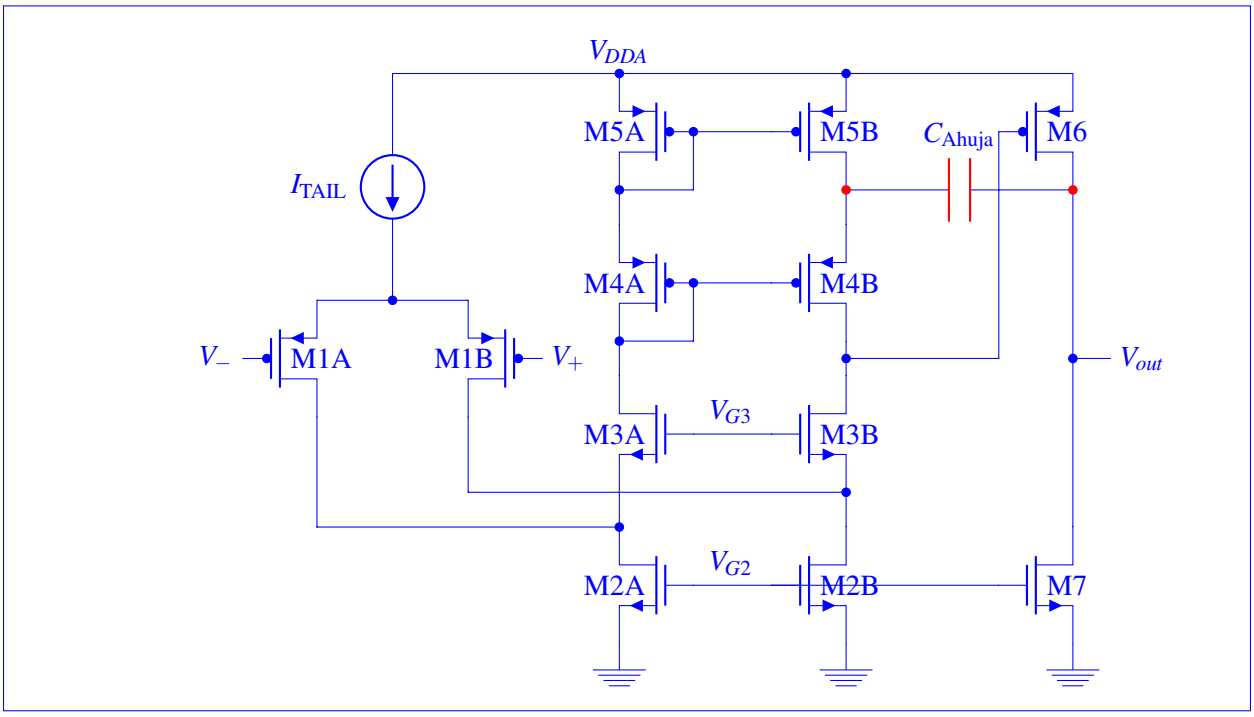
NMOS input pair

iv. What is the absolute minimum open-loop gain necessary to achieve a gain error $\leq 0.5\%$ with a feedback factor of $f = \frac{1}{9}$? You may assume your amplifier is infinitely fast.
Solution: Assuming an infinitely fast amplifier

$$\varepsilon_{\text{gain}} = \frac{1}{A_0 f}$$
$$A_0 \geq 1800 \frac{\text{V}}{\text{V}}$$

$A_0 \geq 1800\text{V/V}$

v. Suppose you use the following topology and would like to use Ahuja compensation for your op amp. Draw the Ahuja compensation capacitor in the diagram below.
Solution:

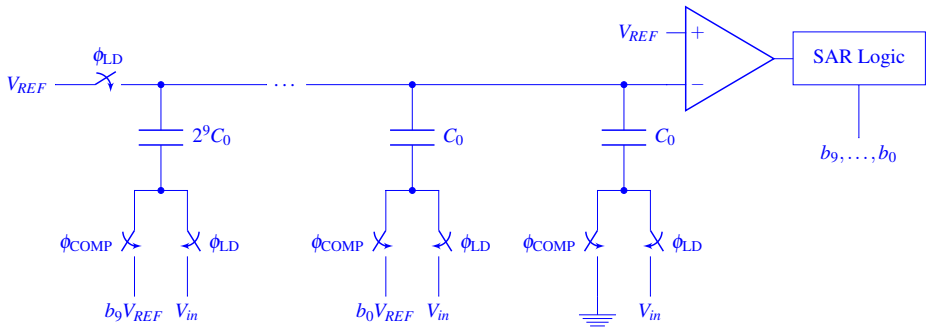


11. Add More Bits! (16 Points)

$V_{in} \in [0,1]$V. The reference voltage is $V_{REF} = 1$V. The analog supply is $V_{DDA} = 1.2$V.

(a) Draw a schematic of a 10-bit ADC using an op amp symbol for the comparator, transistors, capacitors, and the 10-bit digital SAR controller supplied to you (a black box). Don't draw anything for bits 1 through 8, but do draw bits 0 and 9.

Solution:



the switches are all transmission gates (same as in the mux drawing)

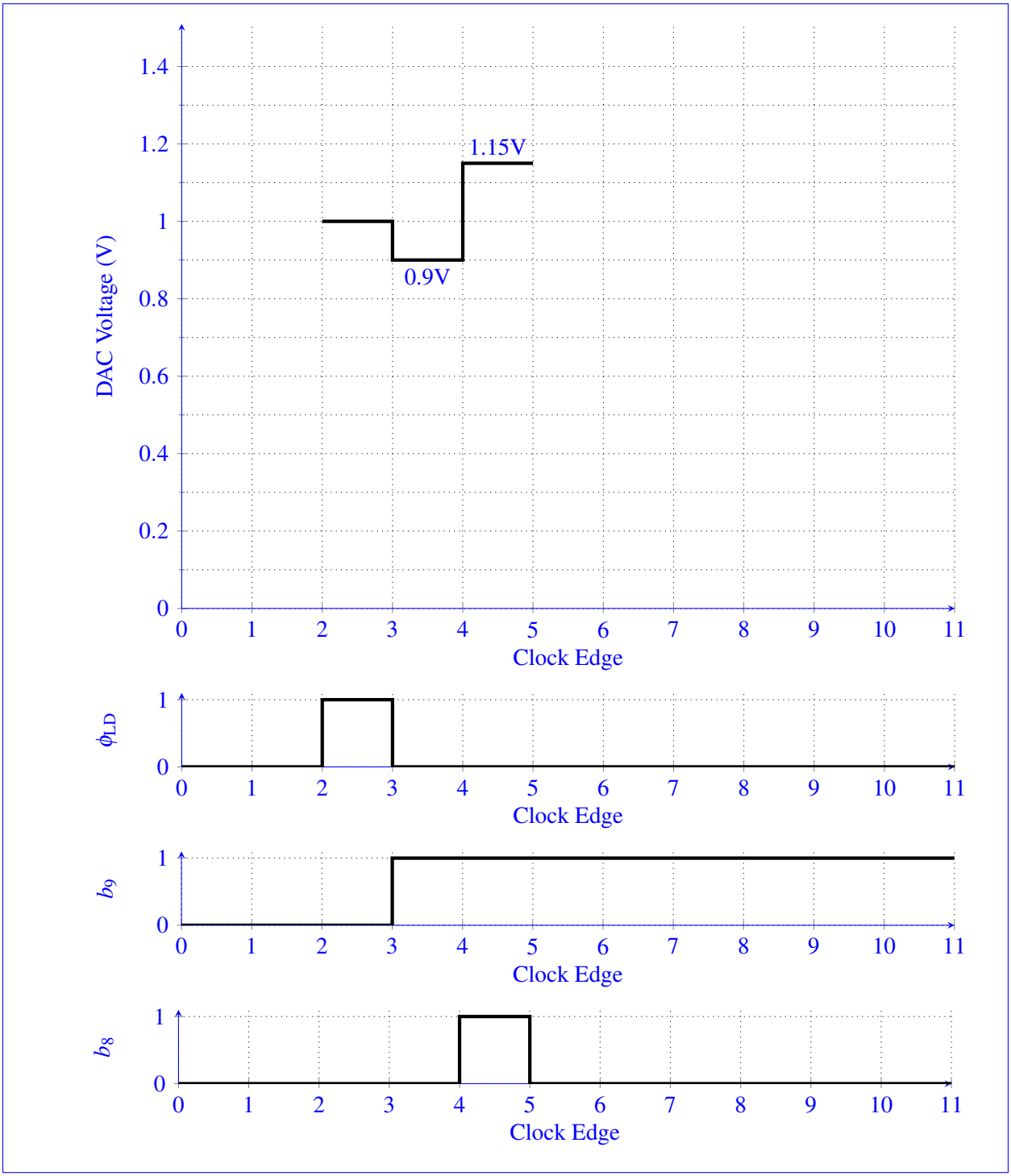
(b) If the unit capacitance is 4fF, what is the total capacitance of the 10-bit ADC (not including any parasitics)?

Solution:

$$4\text{fF} \times 2^{10} = 4096\text{fF} = 4.096\text{pF}$$

(c) Sketch the waveforms for the first two bit decisions (b_9 and b_8) for an input of 0.6V. Specifically, sketch LD, b_9 and b_8 on the lower axes, and sketch the output of the capacitive DAC on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.

Solution:



(d) Comparators aren't free! The comparator now has a parasitic input capacitance of C_p to ground which is $2^8\times$ the DAC's unit capacitance.

Sketch the waveform for the first bit decision b_9 for an input of 0.6V. Specifically, sketch LD, b_9 and b_8 on the lower axes, and sketch the output of the capacitive DAC on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.

Solution: