EE 140/240A Linear Integrated Circuits
Spring 2020 Final

Name	
SID	

Question	**Point Value**
Feed This Way and That	/5
3-Terminal Tater	/6
Single Pole Amp Table	/12
MOSFET Small Signal	/12
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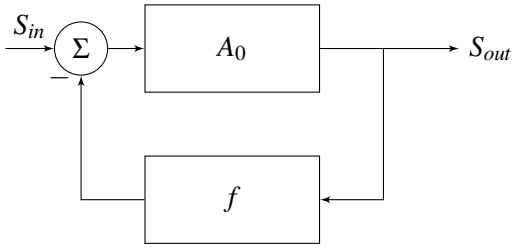
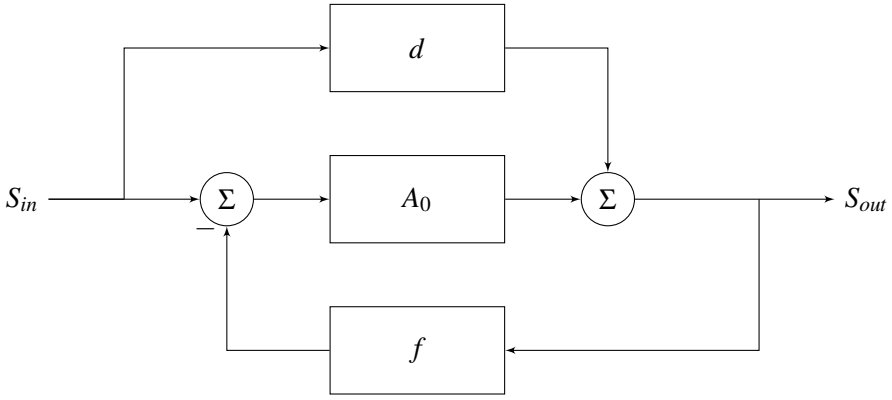
2-Input Mux	/8
PGA Gain 1 or 8	/14
Add More Bits!	/16
Total	/129

1. Feed This Way and That (5 Points)



(a) For the system above, find $\frac{S_{out}}{S_{in}}$



(b) For the system above, find $\frac{S_{out}}{S_{in}}$

2. 3-Terminal Tater (6 Points)

You are given a device with the following equation for its output current:

$$I_{out} = \frac{1}{3}\alpha(V_{in})^3 + \frac{1}{2}\beta(V_{out})^2$$

(a) What is the output resistance R_o of the device?

(b) What is the transconductance G_m of the device?

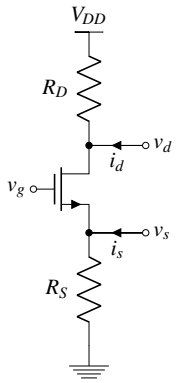
(c) What is the intrinsic small-signal voltage gain of the device? Mind your signs!

3. Single Pole Amp Table (12 Points)

Fill in the following table without a calculator for a single-pole amplifier

A_{v0} (V/V)	ω_p (rad/s)	ω_u (rad/s)	g_m (1/Ω)	r_o (Ω)	C_L (F)
1000	1M				1p
	1M	0.1G		100k	
		10G		1M	20f
	10	10M			100p

4. MOSFET Small Signal Transconductances and Impedances (12 Points)



Find the following small signal values for the single-transistor amplifier above. **Your final answers should have the full, unsimplified expression**

(a) $\frac{i_d}{v_g}$ given $v_d = 0\text{V}_{\text{AC}}$. This is the G_m of a degenerated common source.

(b) $\frac{v_d}{i_d}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source-degenerated common source.

(c) $\frac{v_d}{v_g}$ assuming $R_D = \infty\Omega$. This is the voltage gain of a degenerated common source amplifier.

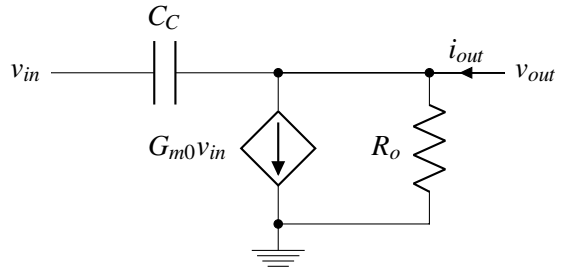
(d) $\frac{i_s}{v_g}$ given $v_s = 0\text{V}_{\text{AC}}$. This is the G_m of a source follower.

(e) $\frac{v_s}{i_s}$ given $v_g = 0\text{V}_{\text{AC}}$. This is the R_o of a source follower.

(f) $\frac{v_s}{v_g}$ assuming $R_S = \infty\Omega$. This is the voltage gain of a source follower.

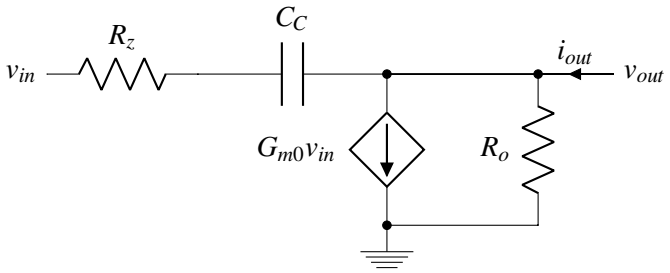
5. Compensation Has Consequences (10 Points)

(a) Calculate the $G_m(s)$ of the following circuit:



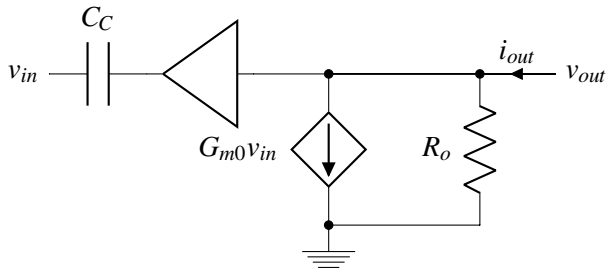
(b) What are the locations of the poles and zeros (if any)? Be sure to specify if they're in the right or left half of the s-plane.

(c) Your colleague proposes the following modification to the previous diagram:



What are the locations of the poles and zeros (if any) of $G_m(s)$? Be sure to specify if they're in the right or left half of the s-plane.

(d) Calculate the $G_m(s)$ of the following circuit assuming the buffer is ideal (infinite input impedance, zero output impedance):

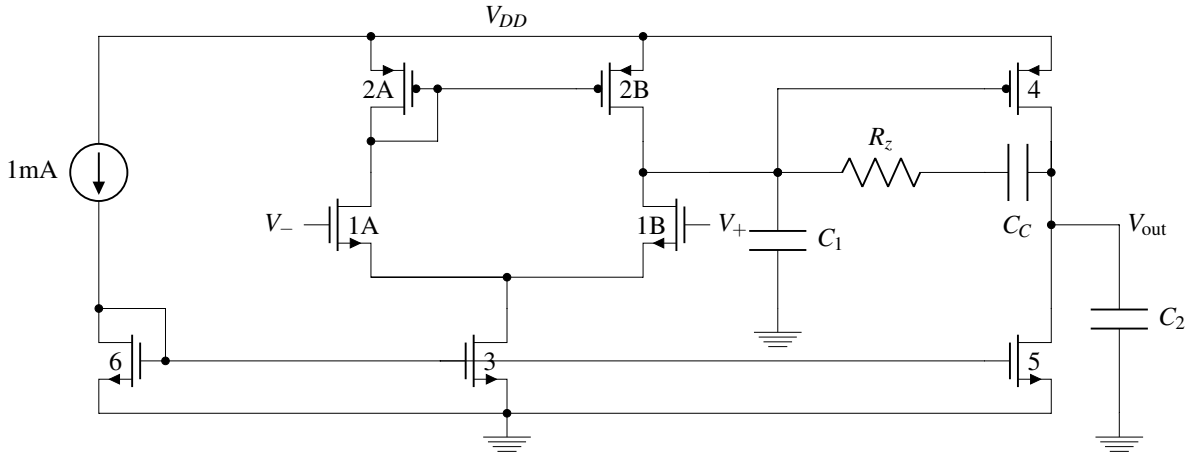


(e) What are the locations of the poles and zeros (if any) of $G_m(s)$? Be sure to specify if they're in the right half or left half of the s-plane.

6. Two Stage Drills (24 Points)

Unless otherwise indicated, you may make the following assumptions:

- All transistors are biased in saturation with $V_{ov} = 0.2\text{V}$
- $V_{DD} = 3\text{V}$, $V_{tn} = -V_{tp} = 1\text{V}$
- M3 and M6 are identical. M5 is $5\times$ wider
- All capacitors are assumed to be zero except C_C, C_1, and C_2



(a) What is the common mode input voltage range (min and max)?

(b) What is the output voltage swing (min and max)?

(c) If $C_1 = 0$, $C_2 = 1\text{pF}$, and $C_C = 1\text{pF}$, what is the positive slew rate in $\frac{\text{V}}{\text{s}}$?

(d) If $C_1 = 0\text{F}$, $C_2 = 10\text{pF}$, and $C_C = 1\text{pF}$, what is the negative slew rate in $\frac{\text{V}}{\text{s}}$?

(e) If $C_1 = 0\text{F}$, $C_2 = 1\text{pF}$, and $C_C = 100\text{pF}$, what is the negative slew rate in $\frac{\text{V}}{\text{s}}$?

A different amplifier with the same topology has the following parameters. You may ignore the pole/zero doublet from the mirror.

$g_{m1,2}$	R_{o1}	g_{m4}	R_{o2}	C_1	C_C	C_2
1mS	10MΩ	1mS	100kΩ	1pF	0.1pF	100pF

(f) If $C_C = 0$F for this part only (magically we will assume no C_{gd4}), what are the uncompensated pole locations?

(g) What is the location of the right-half plane zero?

All plots are on the following pages. Don't forget the last parts of the question!

(h) Plot the magnitude of the second stage gain

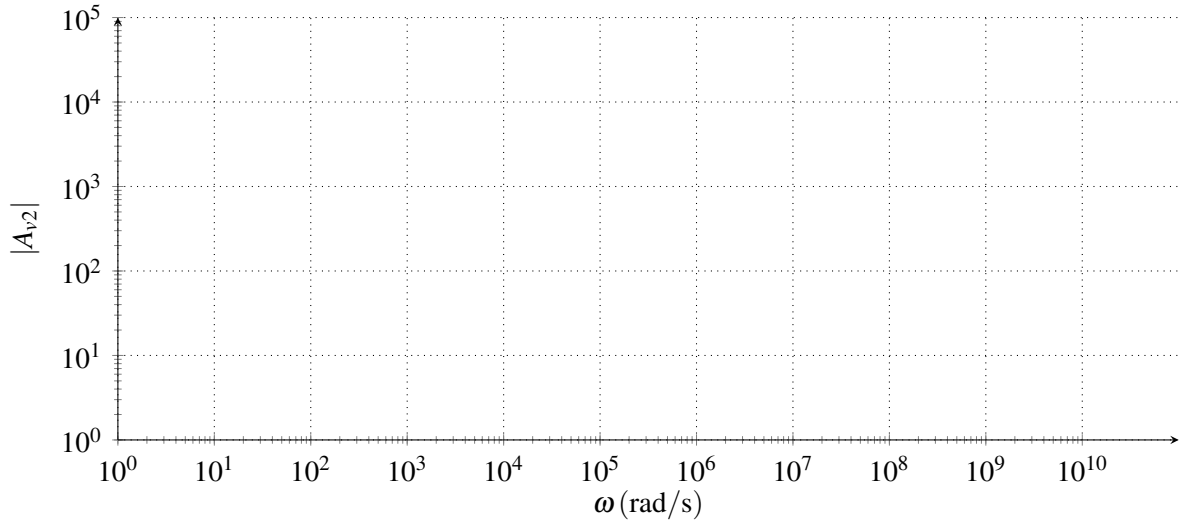
(i) Plot the overall impedance seen at the first stage output including R_{o1}, C_1, C_C, and any effects of Miller multiplication.

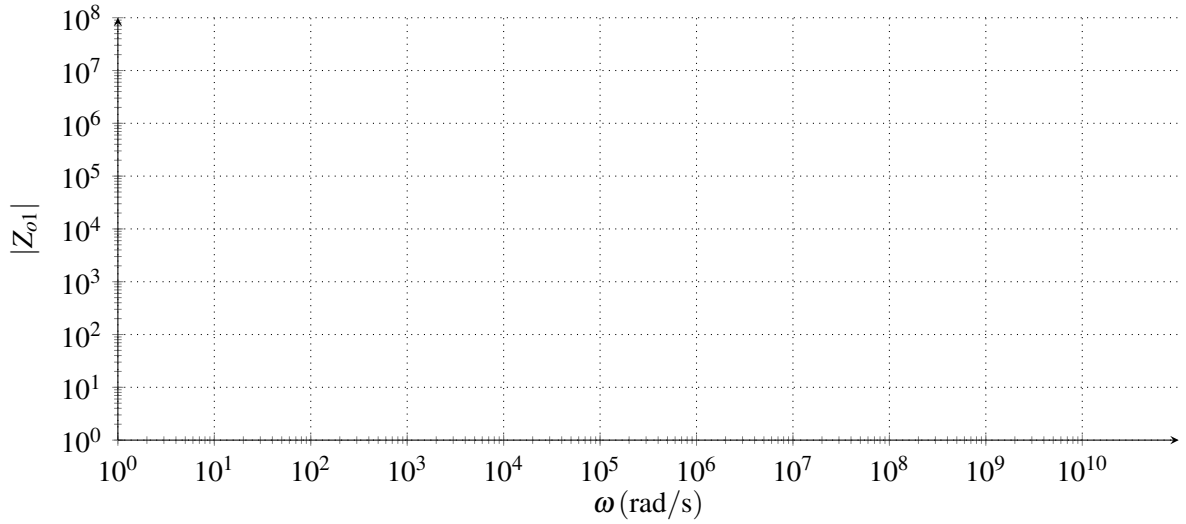
(j) Plot the magnitude of the first stage gain.

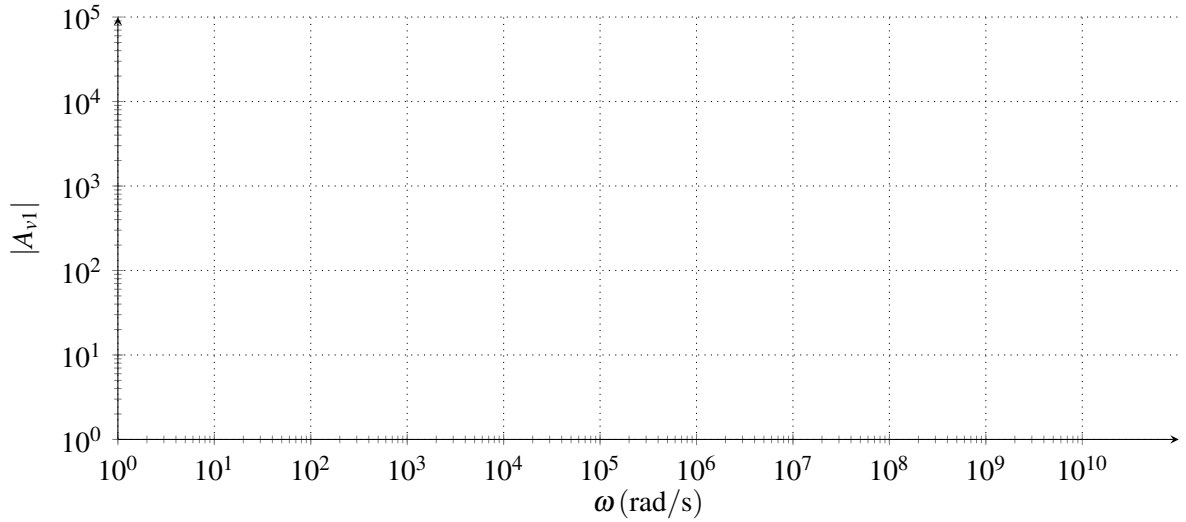
(k) Plot the magnitude and phase of the overall gain. **Label any poles and zeros clearly.**

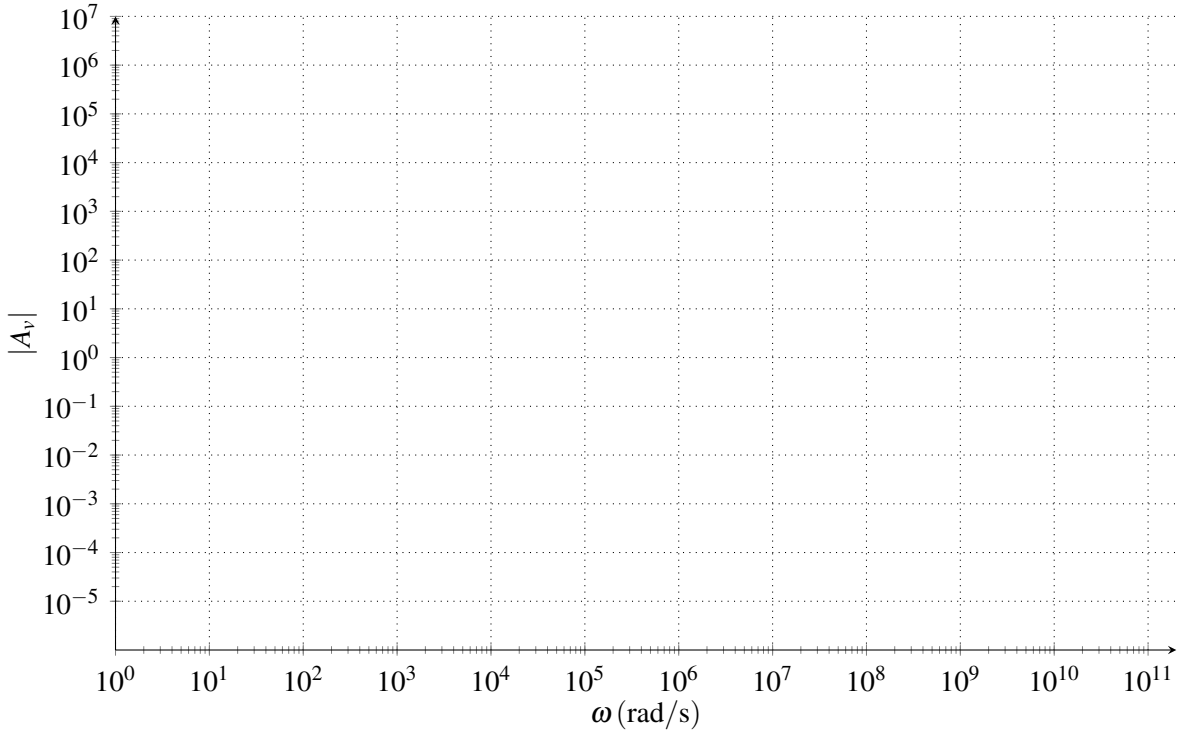
(l) Estimate the unity gain phase margin for this value of C_C.

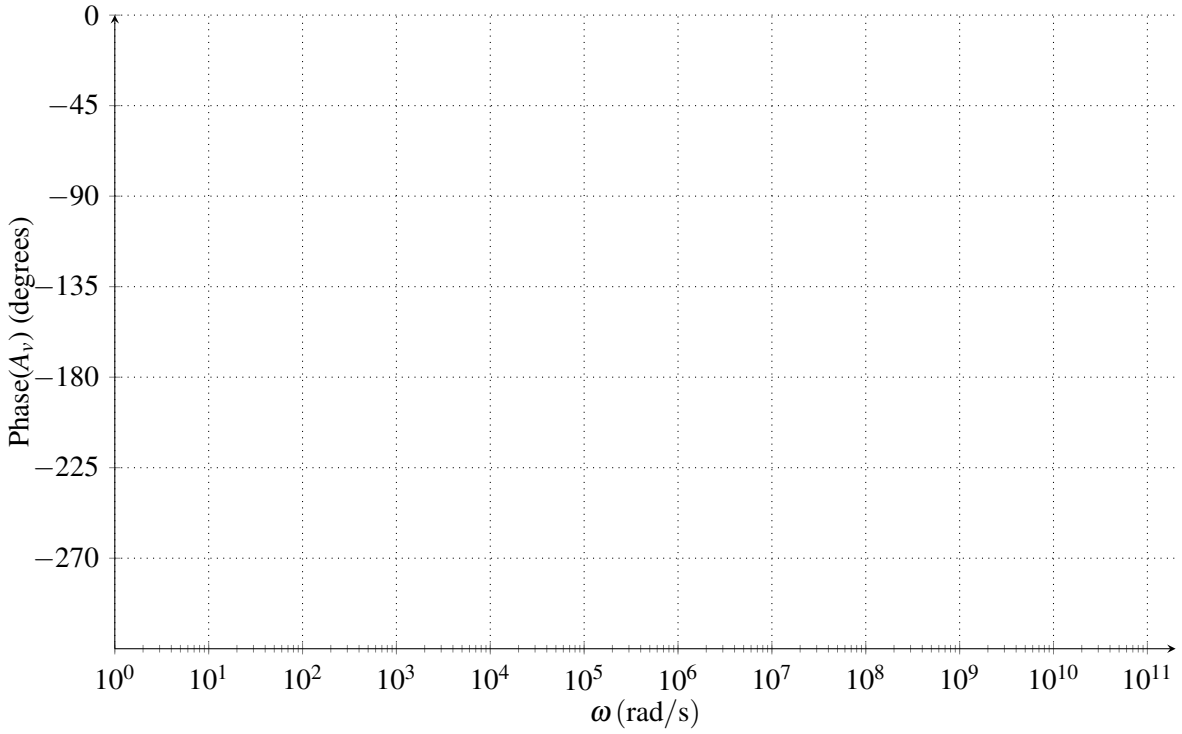
(m) What is the maximum feedback factor and closed-loop gain for which the amplifier has a 45° phase margin?


$|A_{v2}|$
10^0 10^1 10^2 10^3 10^4 10^5
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
ω (rad/s)


$|Z_{o1}|$
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
ω (rad/s)


$|A_{v1}|$
10^0 10^1 10^2 10^3 10^4 10^5
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
ω (rad/s)

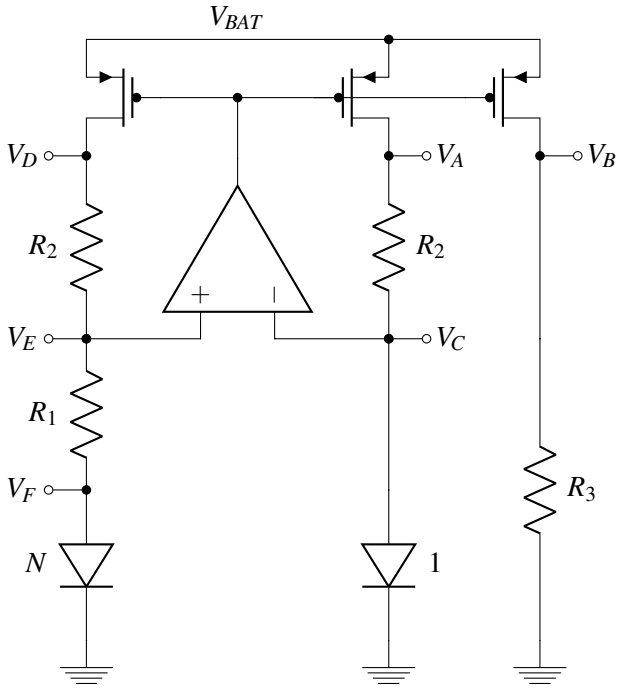




Don't forget the last parts of this question!

7. Bandgap, Revisited (8 Points)

You're given the following bandgap. You may assume it's functioning exactly as intended, that the amplifier is ideal, and that $\lambda = 0\text{V}^{-1}$ for the MOSFETs.



Indicate if the following are PTAT, CTAT, or independent of temperature.

Output	PTAT/CTAT/T-independent?
V_A	
V_B	
V_C	
V_D	
V_E	
V_F	
$V_E - V_C$	
$V_E - V_F$	

8. Regulate Yoself (14 Points)

(a) You are given a battery $V_{BAT} = 1.6$V, a bandgap reference voltage $V_{BG} = 1.2$V, and devices with $V_{tn} = |V_{tp}| = 800$mV. In the box below, draw the schematic for the following. If you use any resistors, clearly indicate their ratios.

i. analog regulator (1.2V)

ii. digital regulator (1.5V)

iii. ADC reference regulator (1V)

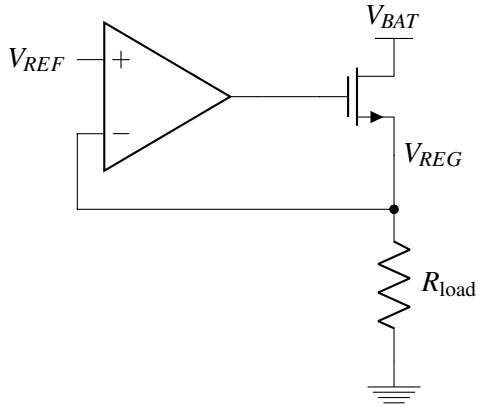
(b) For the analog regulator op amp

i. What is the common mode input?

ii. What is the bare necessity for output swing?

iii. Which of the following will *not* work? {N/P input}, {5T, current mirror amp, 2-stage common source, folded cascode, 2-stage folded cascode}

(c) Your project partner wants you to verify that the regulator they've made below is stable. The op amp has a differential gain of A_{OL}, and you know the MOSFET's small signal parameters g_m and r_o. Find the magnitude of the loop gain $|T| = A_0 f$ of the regulator.



9. 2-Input Mux (8 Points)

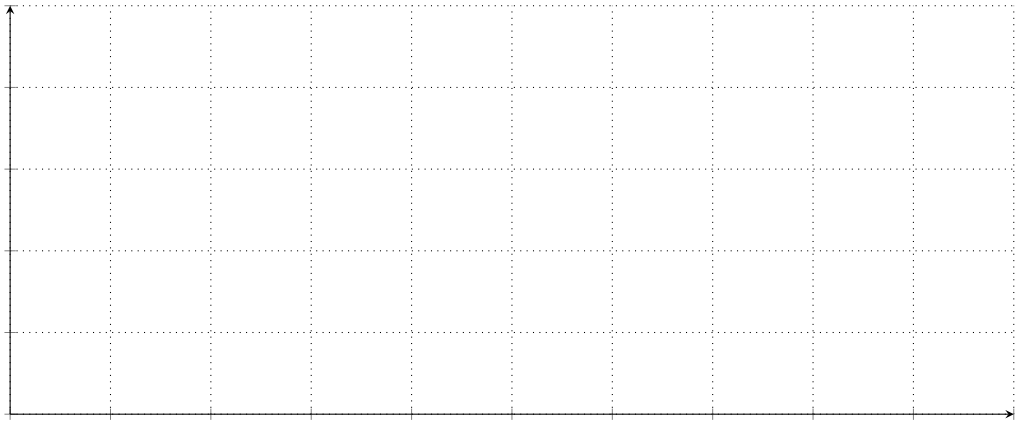
For the following 2-input mux, the input voltage can range from 0V to 1V and the control/select bit is in the V_{DDA} power domain (0, 1.2)V.

(a) Draw the schematic of a 2-input mux using transistors. If you need a digital logic cell, draw the transistor schematic.

(b) Assuming the following, estimate the mux's on-resistance R_{on} for an input near 0V. **Give a numerical value, not just an equation!**

- Every transistor has $W/L = 1.8\mu m/180nm$
- $V_{tn} = -V_{tp} = 0.4V$
- $\mu_n C_{ox} = 2\mu_p C_{ox} = 200\frac{\mu A}{V^2}$

(c) The mux is driving a 100fF capacitor and has one input at 0.1V and another at 0.4V. Carefully sketch the voltage waveform when the input to the mux select switches from the 0.4V input to the 0.1V input. Label the axes. Label the times when the settling accuracy is at 95% and 99.9%.



10. PGA Gain 1 or 8 (14 Points)

(a) Draw the schematic of a PGA with gain settings of 1 **or** 8. You may use an op-amp symbol, transistors, and capacitors. Assume that the gain control bit G and two non-overlapping clock phases ϕ_1 and ϕ_2 are in the analog power domain (0, V_{DDA}). If you need a digital gate, draw the schematic using transistors.

(b) For the op amp,

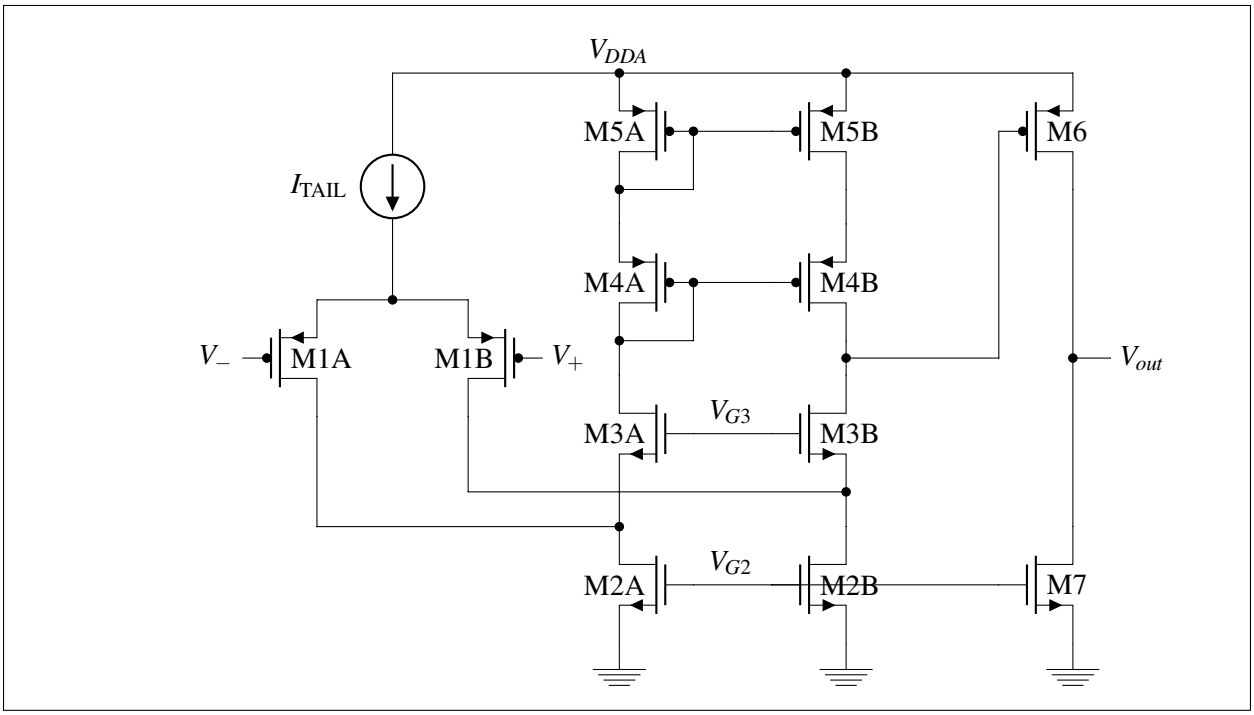
i. What is the common-mode input?

ii. If this PGA is feeding into an ADC with a $V_{REF} = 1\text{V}$, what is the output swing needed?

iii. What type of input pair will *not* work?

iv. What is the absolute minimum open-loop gain necessary to achieve a gain error $\leq 0.5\%$ with a feedback factor of $f = \frac{1}{9}$? You may assume your amplifier is infinitely fast.

v. Suppose you use the following topology and would like to use Ahuja compensation for your op amp. Draw the Ahuja compensation capacitor in the diagram below.



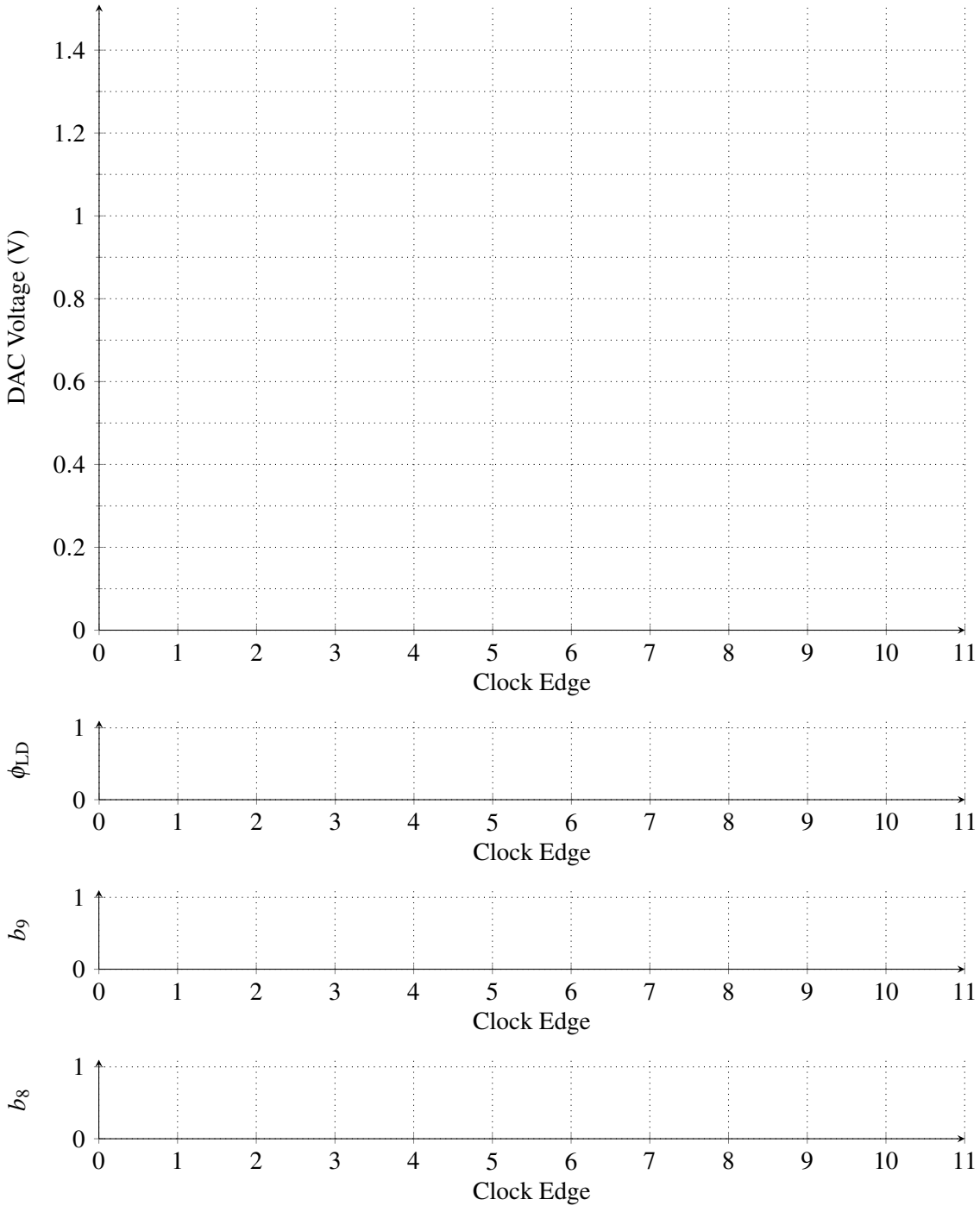
11. Add More Bits! (16 Points)

$V_{in} \in [0,1]$V. The reference voltage is $V_{REF} = 1$V. The analog supply is $V_{DDA} = 1.2$V.

(a) Draw a schematic of a 10-bit ADC using an op amp symbol for the comparator, transistors, capacitors, and the 10-bit digital SAR controller supplied to you (a black box). Don't draw anything for bits 1 through 8, but do draw bits 0 and 9.

(b) If the unit capacitance is 4fF, what is the total capacitance of the 10-bit ADC (not including any parasitics)?

(c) Sketch the waveforms for the first two bit decisions (b_9 and b_8) for an input of 0.6V. Specifically, sketch LD, b_9 and b_8 on the lower axes, and sketch the output of the capacitive DAC on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.



(d) Comparators aren't free! The comparator now has a parasitic input capacitance of C_p to ground which is $2^8\times$ the DAC's unit capacitance.

Sketch the waveform for the first bit decision b_9 for an input of 0.6V. Specifically, sketch LD, b_9 and b_8 on the lower axes, and sketch the output of the capacitive DAC on the upper axes. Clock edges correspond to the vertical dotted lines. LD goes high on the second rising edge.