50s	1
40s	6
30s	4
20s	1
10s	2

Midterm 1 $\mu = 37$, $\sigma = 11$

Midterm 2 - probably paper

Op-amps

What operations?

structure

LM324

CMOS 2 stage.

"mathematical operation" amplifier

1940s anti-aircraft artillery M-9 gun director

Parkinson

1952 K2-W $A_0 = 20{,}000$

$ 22 $\omega_u = 2\,\text{Mrad/s}$

Philbrick $\pm 50\,V$ swing into $50\,k\Omega$

$150\,V$ plate-to-cathode

$I_p = 300\,\mu A$, $I_g = 10\,nA$

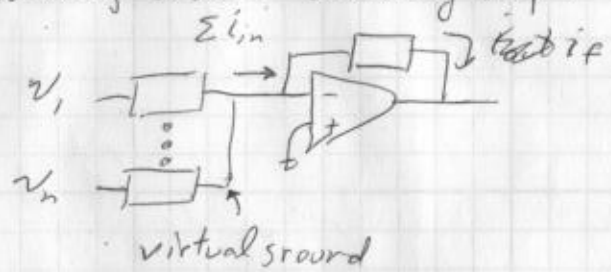
V_{os} $-1.5 \pm 0.25\,V$

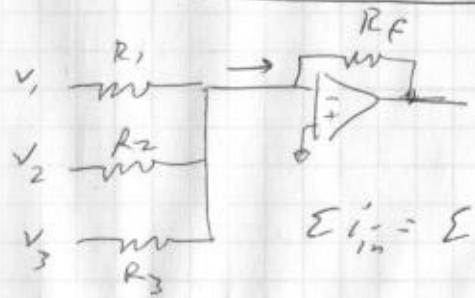
V_{sup} $\pm 300\,V$

Apollo
Nike
EE128 before ≈ 1980 } analog computation

How do you simulate a differential equation?

Building block: summing amp.





$$\Sigma i_{in} = \Sigma \frac{v_i}{R_i}$$

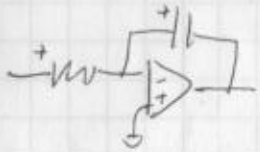
$$v_o = -R_F i_F = -R_F \Sigma \frac{v_i}{R_i}$$

V_i inputs could be from other mathematical operations

140/240 20sp W6L1

$$i_{in} = C\frac{dv_i}{dt}$$

$$V_o = -R_f C \frac{dv_i}{dt}$$



$$i_{in} = \frac{v_i}{R}$$

$$V_o = -\int_0^t \frac{i_{in}}{C}\,d\tau = -\int_0^t \frac{v_i}{RC}\,d\tau$$

t=0 when voltage was reset

"integrator wind-up"

can solve any linear ODE

EE128 lab

Apollo

countless weapons systems

Non-linear

$$i_{in} = I_s e^{\frac{V_i}{V_{TH}}}$$

$$V_o = -R_F I_s e^{\frac{V_i}{V_{TH}}}$$

$$V_o = V_{th} \ln\left(\frac{V_i/R}{I_s}\right)$$

With a log table, even adders can multiply

$$A \cdot B = \exp(\ln A + \ln B)$$

④ ① ③ ②

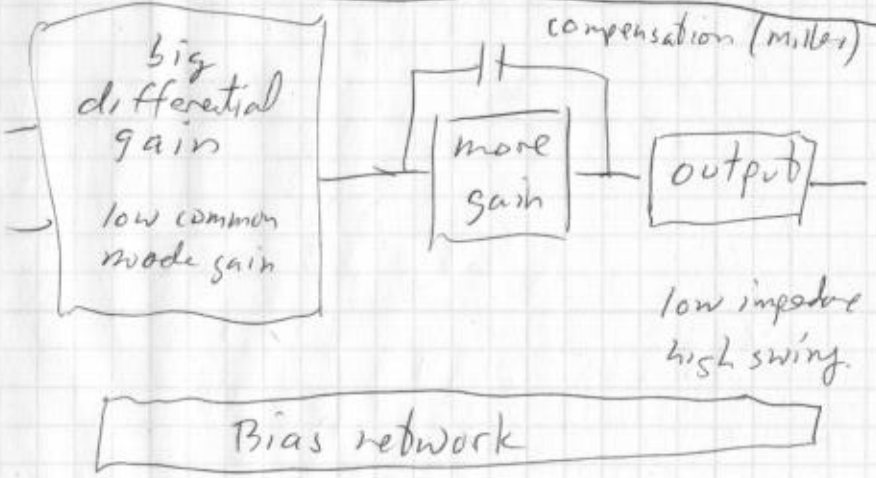
4 operations

4 op-amps

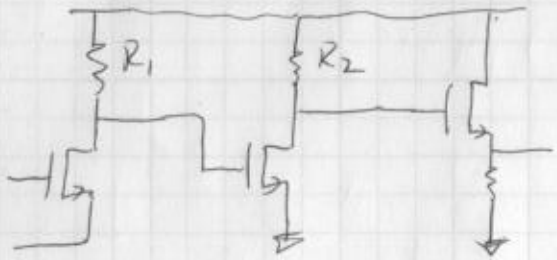
initially tubes, then NPN, then integrated NPN 1970s

NPN + PNP

integrated PMOS, NMOS, CMOS



Simplest (terrible)

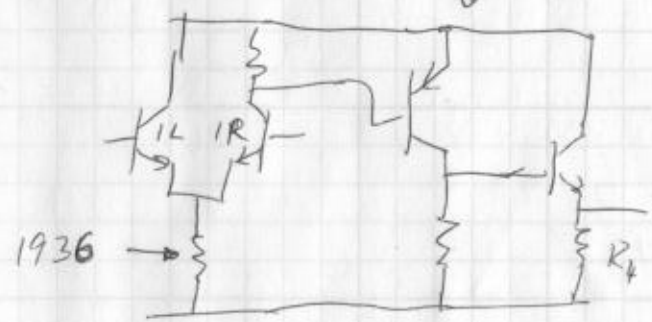


diff gain gain low impedance

bad input offset, input resistance, gain, swing, etc.

Better

Q: why PNP? A: Bias, swing

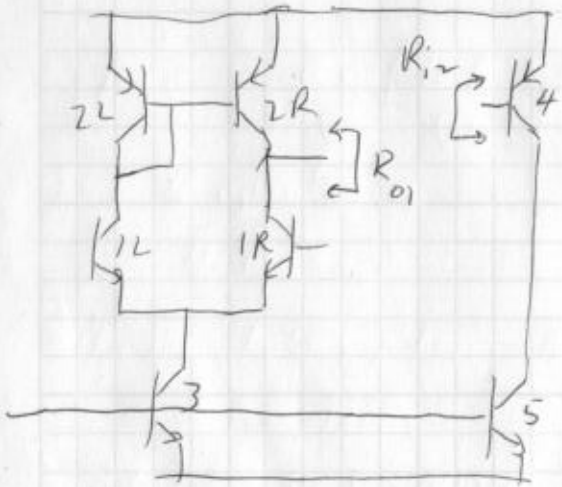


$\frac{1}{g_m} \| R_4$

$\approx ?$

$\frac{V_{TH}}{I_c} \| \frac{V_0}{I_c} \approx \frac{V_{TH}}{I_c}$

Better



$R_{01} = r_{01R} \| r_{02R}$

$\cong \frac{V_A}{2I_c}$

$R_{i2} = \frac{\beta}{g_m} = \frac{\beta V_{TH}}{I_c}$

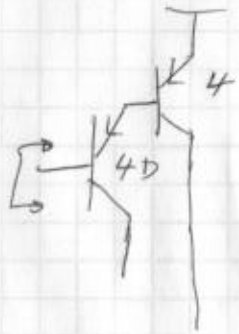
compare $\frac{V_A}{2}$, βV_{TH}

10x to 100x gain loss?

V_{01} bias $V_{01} = V_{CC} - V_{BE,on2}$

$V_{\ldots}$ ~ same

increase input resistance: Darlington



$I_{C4D} \approx I_{B4} = \frac{I_{C4}}{\beta_4}$

$r_{\pi 4D} = \frac{\beta_{4D}}{g_{m4D}} = \frac{\beta_{4D} V_{TH}}{I_{C4D}}$

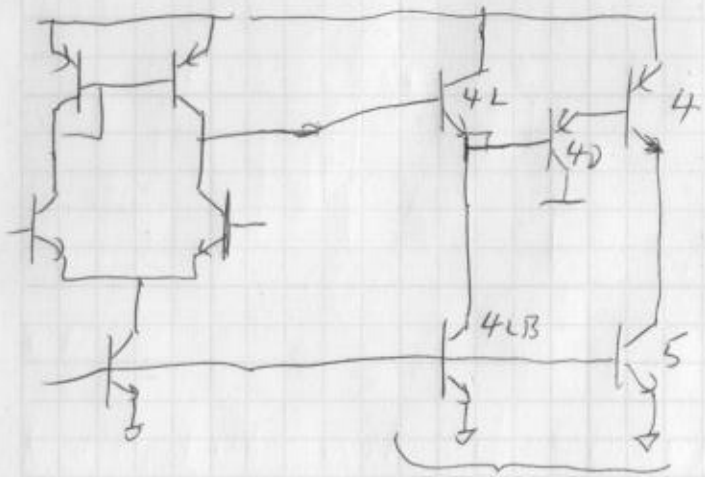
$= \frac{\beta_4 \beta_{4D} V_{TH}}{I_{C4}}$

$\beta_4 \beta_{4D} V_{TH}$ probably comparable to V_A

but now $V_{I2} = V_{CC} - V_{BE\,on\,4} - V_{BE\,on\,4D}$

$\Rightarrow$ input offset

add an NPN V_{BE} to bring V_{IL} back up



≈ upside down LM324

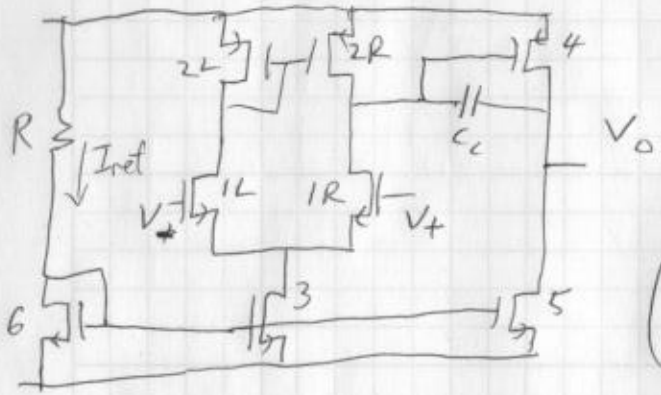
input impedance: r_π too low

add Darlingtons

βr_π better

sense input current and subtract it!

CMOS 2 stage



Diff pair 1LR

active load 2LR

gain stage 4
4,5

bias network 3,5,6

signal path 1LR
2LR
3

Complementary

Find: Diff gain
common mode gain

input common mode range
output swing

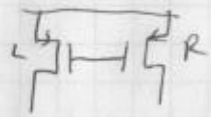
output current drive
slew rate

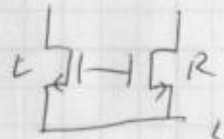
frequency response

power supply rejection ratio

noise

current mirrors





Q: if $\frac{W}{L}$ (both W, L) same

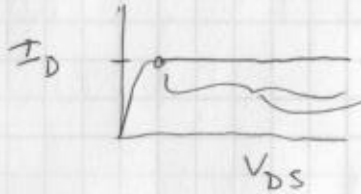
V_t, μC_{ox} same

V_S, V_G same

and $\lambda = 0$, how different can I_D L, R be?

~~and both in~~ both V_D in saturation

A: not at all different.



both must be on this flat part of the curve

if $\lambda \neq 0$?

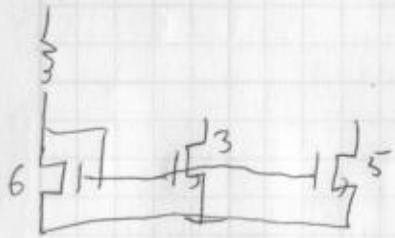
Depends on drain voltage

$$\frac{\Delta I_D}{I_D} = \frac{\frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2\left[(1+\lambda V_{DS1})-(1+\lambda V_{DS2})\right]}{\frac{\mu C_{ox}}{2}\frac{W}{L}V_{ov}^2(1+\lambda V_{DS})}$$

$$= \frac{\lambda \Delta V_D}{1+\lambda V_{DS}} \approx \frac{\Delta V_D}{V_A}$$

e.g. $\lambda = \frac{1}{10V}$, $\Delta V_D = 1V$

$\Delta I_D = 10\% I_D$



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{ov}^2(1+\lambda V_{DS})$$

same for all 3

possibly different.

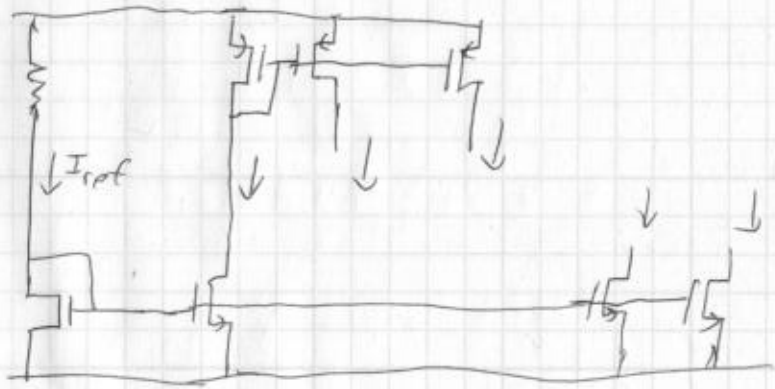
to vary $\frac{W}{L}$

make integer ratios (copies of same base transistor)

can still have rational fractions

$\left(\frac{W}{L}\right)_6 = N\left(\frac{W}{L}\right)_0$ $\left(\frac{W}{L}\right)_3 = M\left(\frac{W}{L}\right)_0$ $\frac{I_{D3}}{I_{D6}} \approx \frac{M}{N}$

to get sources and sinks, mirror to top



longer channels a good idea