1. Bangap

A particular diode D1 has a saturation current of 0.01pA, and at 100µA current at room temperature the diode voltage has a temperature coefficient of $-1.5\text{mV/K}$. You are using copies of this diode to make a bandgap reference, with D2 composed of 100 copies of D1. Assuming that the current in both diodes is maintained at 100µA at room temperature,

**Rubric:** (6 Points)
- +2 for parts a, b, d, e no partial credit.
- +3 for part c.
- +9 for part f, +3 per line/function
- +2 for part g.

(a) What is the voltage on D1 at room temperature?

**Solution:** Between 0.01pA and 100µA there are 10 decades, and at 60mV/decade,

\[
\begin{align*}
\text{600mV}
\end{align*}
\]

(b) What is the voltage on D2 at room temperature?

**Solution:** The voltage is \(\ln(100)\frac{keT}{q}\) lower than that across D1, so
(c) What is the difference between the two diode voltages at 200K, 300K, and 400K?

**Solution:** The difference scales with \( V = \frac{k_B T}{q} \)

\[
\begin{align*}
@200K & : 80mV \\
@300K & : 120mV \\
@400K & : 160mV
\end{align*}
\]

(d) What is the temperature coefficient of the voltage on D2?

**Solution:**

\[
\begin{align*}
V_{D2} & = V_{D1} - \ln(100) \frac{k_B T}{q} \\
\frac{\partial V_{D2}}{\partial T} & = \frac{\partial V_{D1}}{\partial T} - \ln(100) \frac{k_B}{q} \\
& = -1.5 \frac{mV}{K} - \frac{120mV}{300K} \\
& = -1.9 \frac{mV}{K}
\end{align*}
\]

(e) Roughly what is the right value for \( R_1 \)?

**Solution:**

From feedback, we know \( V_A = V_B \), and we’re given the current value of 100µA. At room temperature,

\[
R_1 = \frac{V_{D1} - V_{D2}}{I} = \frac{1,200\Omega}{1}
\]

\[ R_1 = 1,200\Omega \]

(f) On the next page, carefully sketch by hand the voltage on D1, the voltage on D2, and the difference between them as a function of temperature from 200K to 400K.

(g) On the same plot, if \( R_3 = R_2 = 4R_1 \), sketch \( V_{ref} \) vs. temperature from 200K to 400K.
Solution:

\[
V_{REF} = V_{D1} + IR_2 \\
= V_{D1} + \frac{V_{D1} - V_{D2}}{R_1} R_2 \\
= V_{D1} + (V_{D1} - V_{D2}) \frac{R_2}{R_1}
\]

Because tikz doesn’t seem to like it when I try to do math while plotting sometimes, here’s a table of values:

<table>
<thead>
<tr>
<th>Temperature</th>
<th>200K</th>
<th>300K</th>
<th>400K</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{D1}$</td>
<td>750mV</td>
<td>600mV</td>
<td>450mV</td>
</tr>
<tr>
<td>$V_{D2}$</td>
<td>670mV</td>
<td>480mV</td>
<td>290mV</td>
</tr>
<tr>
<td>$V_{D1} - V_{D2}$</td>
<td>80mV</td>
<td>120mV</td>
<td>160mV</td>
</tr>
<tr>
<td>$V_{REF}$</td>
<td>1,070mV</td>
<td>1,080mV</td>
<td>1,090mV</td>
</tr>
</tbody>
</table>
2. Early Op Amp Check out the “early op-amp” figure from Maxim Integrated (included below for convenience)

![Early Op Amp Diagram]

Figure 1: Source: [https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428](https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428)

(a) Circle and label the following components:
   i. differential pair with resistive load
   ii. tail current sink
   iii. common emitter gain stage with level-shifting diodes
   iv. output stage with current-limiting resistors
   v. Zener diode based voltage reference

**Solution:**

![Solution Diagram]

**Rubric:** (5 Points)
(b) Why is there a resistor in series with the Zener diode?

**Solution:**

The series resistor supplies current to the zener to run it in reverse breakdown, also limits current through the Zener diode.

**Rubric:** (1 Points)

• +1: Series resistor limits current (saying that it supplies current to the Zener so it runs in reverse breakdown is also acceptable).

(c) If the Zener has a reverse breakdown of 3.5V, and the tail resistor is 1kΩ, what is the tail current? Does it vary much with supply voltage?

**Solution:**

\[ I_{\text{T A I L}} = \frac{V_{\text{Zener}} - V_{\text{BE}}}{R_{\text{T A I L}}} \]

\[ = \frac{3.5 - 0.7}{1000} \]

\[ \approx 2.8 \text{mA} \]

\[ I_{\text{T A I L}} \approx 2.8 \text{mA} \]

Neither \( V_{\text{Zener}} \) nor \( V_{\text{BE}} \) depend on the supply voltage, hence, the tail current is relatively independent of supply.

**Rubric:** (2 Points)

• +1: Correct calculation of tail current
• +1: Correct explanation of no dependence on supply voltage

(d) If you were going to add a compensation capacitor to this op-amp, where would you put it? (draw it on the circuit)

**Solution:**

See (a).

**Rubric:** (1 Points)

• +1: Correct placement of compensation capacitor. Placement from the input of the common emitter to the output is also acceptable.

3. LM324

Take a look at the datasheet for the TI LM324 quad op-amp. [http://www.ti.com/lit/ds/symlink/ lm324.pdf](http://www.ti.com/lit/ds/symlink/lm324.pdf) TI has been selling this op-amp for more than 40 years! (they are 10 cents each on DigiKey).

From Figure 4 on the LM324 datasheet
(a) Estimate the slew rate in positive and negative slewing when the output load is 50pF.

**Solution:**

Copied from the datasheet, we're told that a load of 50pF was attached:

\[
\text{falling slew rate} \approx -\frac{1.75\text{V}}{5\mu\text{s}} = -0.35\frac{\text{V}}{\mu\text{s}}
\]

\[
\text{rising slew rate} \approx \frac{2.25\text{V}}{5\mu\text{s}} = 0.45\frac{\text{V}}{\mu\text{s}}
\]

**Rubric:** (4 Points)

- +1: Correct method for calculating positive slew rate
- +1: Correct method for calculating negative slew rate
- +1: Correct numerical positive slew rate
- +1: Correct numerical negative slew rate

(b) We haven’t studied output stages, but you can find the output current limits in the table on page 7. Is the slew rate due to the output capacitor? (Hint: No. Explain why.)

**Solution:**

The minimum output stage current is 1mA. Thus, the slew rate limit of the output stage would end up being \(\frac{1\text{mA}}{50\text{pF}} = 20\frac{\text{V}}{\mu\text{s}}\), which is a lot larger than the values we got above!

**Rubric:** (2 Points)

- +1: Calculated the slew rate that would come from the output capacitor
- +1: Correctly concluded with correct reasoning that the output stage does not limit the slew rate
(c) What else could it be then? Estimate the size of the compensation capacitor $C_c$.

**Solution:**

Well we really only have one other thing it could be (the compensation capacitor), which both by the rising and falling edges has a current limit of 6µA from the diff pair current source. Averaging the rising and falling slew rates, we get

\[
C = \frac{I}{\frac{dV}{dt}} \approx \frac{6\mu A}{0.375\frac{V}{\mu s}} \approx 16pF
\]

\[C_c \approx 16pF\]

**Rubric:** (2 Points)

- +1: Indicated the tail current was the limiting factor
- +1: Correct numerical value for $C_c$

4. **LT1008**

The LT1008 ([https://www.analog.com/media/en/technical-documentation/data-sheets/LT1008.pdf](https://www.analog.com/media/en/technical-documentation/data-sheets/LT1008.pdf) also decades old, $3.55$ on DigiKey) is not internally compensated. This gives you higher performance (bandwidth, slew rate) for higher gain, but it means you have to add external capacitance when using the amplifier in low-gain configurations. They give you two choices: either add a capacitor $C_F$ that will be somewhat Millerized or add $C_S$ that looks more like our $C_2$.

(a) With a closed loop gain of 1000 and perfect feedback resistor matching,

i. estimate your gain error at 0.1Hz

ii. estimate the closed-loop pole location with $C_S = 10pF$ vs. $C_F = 30pF$ (page 6, lower left)

**Solution:**

At $f = 0.1Hz$, the DC gain $A_{vo} = 130dB$ and $3.2M$. As closed-loop gain $A_{vc} = 1000$, loop gain $A_f = A_{vo}/A_{vc} = 3.2K$. Then fractional gain error is $1/3.2K = 31.3e^{-3}$. 
For $C_S = 10\,\text{pF}$, open-loop pole is $\omega = 5\,\text{Hz}$. The closed-loop pole is $3.2K \cdot 5 = 16\,\text{kHz}$.

For $C_F = 10\,\text{pF}$, open-loop pole is $\omega = 0.2\,\text{Hz}$. The closed-loop pole is $3.2K \cdot 0.2 = 640\,\text{Hz}$.

**Rubric:** (3 Points)

- +1: Correct gain error
- +1: Per correct pole (2×)

(b) With $C_F = 3\,\text{pF}$ vs. 30\,\text{pF}, what is the maximum feedback factor (and corresponding minimum gain and max bandwidth) that will give a phase margin of 60? (page 6, lower right)

**Solution:**

For $C_F = 3\,\text{pF}$, closed-loop gain $A_{vc} = 25\,\text{dB} \approx 15V/V$. Then, the maximum feedback factor $f = 1/A_{vc} \approx \frac{1}{15}$, with maximum bandwidth 300\,kHz.

For $C_F = 30\,\text{pF}$, closed-loop gain $A_{vc} = 0\,\text{dB} = 1$. Then, the maximum feedback factor $f=1$, with maximum bandwidth 1\,MHz.
Rubric: (4 Points)
- +1: Per correct gain ($2\times$)
- +1: Per correct bandwidth ($2\times$)

5. Amps and Slewing

For each of the following four op-amps, redraw the schematic of the op amp including only those transistors that are on when the op-amp is slewing positive, and then slewing negative (there should be 8 figures: 2 topologies, 2 types of input transistors, 2 slewing directions).

(a) Our standard 5T single stage CMOS op amp with an NMOS input, and with PMOS input

**Solution:**

Devices marked in red are on

Rubric: (12 Points)
- +1: Correct device indicated as on ($12\times$)
(b) The current mirror op-amp with NMOS and with PMOS

**Solution:**

Devices marked in red are on

![Diagram showing negative and positive slewing](image)

**Rubric:** (20 Points)

- +1: Correct device indicated as on (20×)
- -1: Incorrect device indicated as on (minimum 0 points)

6. Two-Stages Slewling

For a two-stage NMOS-input CMOS op-amp with the output stage biased at 100µA and the tail current at 10µA

(a) Calculate the positive and negative slew rate if \(C_c = 1\text{pF}\) and \(C_L = 1\text{pF}\)
**Solution:**

\[ I = C \frac{dV}{dt} \]
\[ \frac{dV}{dt} = \frac{-I}{C} \]

In each case we need to consider the possible causes of slewing. For negative slew rate, we consider two cases and assume \( A_{v2} \gg 1 \):

\[ \frac{-I_{\text{tail}}}{C_c} = -\frac{10 \mu A}{1 \text{pF}} = -10 \times 10^6 \frac{V}{s} \]
\[ \frac{-I_{D5}}{C_L} = -\frac{100 \mu A}{100 \text{pF}} = -1 \times 10^6 \frac{V}{s} \]

We choose the most restrictive of the two (the lecture notes say the minimum of two negative values, but it should be the minimum of the absolute value of the two negative values).

For positive slew rate, the PMOS of the second stage can nominally provide infinite current so long as its gate is driven correctly, so the first stage + compensation capacitor limit the positive slew rate (the compensation cap is Millerized, which removes the gain term that would come from the second stage)

\[ \frac{I_{\text{tail}}}{C_c} = \frac{10 \mu A}{1 \text{pF}} = 10 \times 10^6 \frac{V}{s} \]

**Rubric:** (4 Points)

- +1: Correct positive slew rate equation
- +1: Correct positive slew rate numerical value
- +1: Correct negative slew rate equation
- +1: Correct negative slew rate numerical value

(b) Calculate the positive and negative slew rate if \( C_c = 1 \text{pF} \) and \( C_L = 100 \text{pF} \)

**Solution:** In a similar fashion as before:

\[ \frac{-I_{\text{tail}}}{C_c} = -\frac{10 \mu A}{1 \text{pF}} = -10 \times 10^6 \frac{V}{s} \]
\[ \frac{-I_{D5}}{C_L} = -\frac{100 \mu A}{100 \text{pF}} = -1 \times 10^6 \frac{V}{s} \]

\[ \frac{I_{\text{tail}}}{C_c} = \frac{10 \mu A}{1 \text{pF}} = 10 \times 10^6 \frac{V}{s} \]
positive rate $= 10 \times 10^6 \frac{V}{s}$
negative rate $= 1 \times 10^6 \frac{V}{s}$

Rubric: (4 Points)
• +1: Correct positive slew rate equation
• +1: Correct positive slew rate numerical value
• +1: Correct negative slew rate equation
• +1: Correct negative slew rate numerical value

7. Two-Stage Amp Transient

For a two-stage NMOS-input CMOS op-amp with the output stage biased at 100µA and the tail current at 10µA with $C_C = 1pF$ and $C_L = 100pF$, assume a 5V supply, 1V threshold voltages, and 0.1V overdrive voltages for all transistors. With the op-amp in unity gain feedback,

(a) On a single plot carefully sketch the output voltage of the first and second stage vs. time when the input makes a step change from 2V to 4V. Your plot should clearly show initial and final values, and rates of change. Calculate the rate of change of the voltage on $C_c$. You only need to show the slewing behavior, but estimate the voltage and time at which the op amp stops slewing.

Solution: For the positive slew rate, we know

$$ \left( \frac{dV_{out2}}{dt} \right)_+ \approx \frac{I_{tail}}{C_C} = 10 \frac{V}{\mu s} $$

For the first stage, we suppose we know the gain of the second stage so

$$ \left( \frac{dV_{out1}}{dt} \right)_+ \approx -\frac{I_{tail}}{A_{v2}C_C} $$

where the first stage output starts at $V_{DD} - |V_{tp}| - |V_{ov}| = 3.9V$.

- $V_{out2}$ is blue and has a positive slope of $10 \frac{V}{\mu m}$
- $V_{out1}$ is red and has a negative slope less than that of $V_{out2}$
- $V_{out1}$ starts at 3.9V
As an aside, slewing will stop when the slope of the typical exponential linear response is equivalent to that of the slew rate. If the phase margin is 45°, then we know the time constant of the unity gain feedback circuit will be equal to the unity gain frequency of the entire amplifier at the second pole location:

\[
\frac{g_m}{C_L} = \frac{2I_{out}}{V_{ov}C_L}.
\]

For back-of-the-envelope calculations, you can say that slewing stops when the differential input gets back to \(\sqrt{2}V_{ov}\) in the quadratic model and roughly \(2V_{ov}\) for the velocity saturated model. Give yourself credit if you used an answer like this.

**Rubric:** (4 Points)
- +2: Correct slew rate limiting ratio
- +2: Correct start and end points

(b) Repeat, for an input transition from 4V to 2V

**Solution:** Consider which rate is our limiting factor:

\[
\frac{I_{tail}}{C_C} = 10 \frac{V}{\mu s} \quad \frac{I_{OUT}}{C_L} = 1 \frac{V}{\mu s}
\]

we choose the more restrictive of the two, or \(1V/\mu s\)

![Graph](image)

- \(V_{out2}\) is blue and has a negative slope of \(1 \frac{V}{\mu m}\)
- \(V_{out1}\) is red and has a positive slope less than that of \(V_{out2}\)
- \(V_{out1}\) starts at 3.9V

**Rubric:** (6 Points)
- +2: Identified limiting factor for negative slew rate
- +2: Correct numerical computation given chosen limiting factor
- +2: Correct endpoints

8. Continuing...

If the previous op-amp had an open-loop phase margin of 70°, a gain of 10000, and a pole at 1000rad/s
(a) What is the open-loop unity gain frequency?
   **Solution:** Because the phase margin is over 45°, the system behaves functionally like a single-pole system.
   \[
   \omega_u = A_{v0} \omega_p = 10 \text{Mrad/s}
   \]

(b) What is the closed-loop pole frequency and time constant?
   **Solution:** In unity gain feedback, our pole frequency is pushed out to our unity gain frequency, and the time constant is the reciprocal.
   \[
   \omega_{p,CL} = 10 \text{Mrad/s}
   \]
   \[
   \tau_{CL} = 0.1 \mu s
   \]

(c) If the desired settling error is 0.1mV, how many time constants are needed to settle?
   **Solution:** It helps to put things in terms of percentages/fractions:
   \[
   \frac{0.1 \text{mV}}{(4 - 2) \text{V}} = 5 \cdot 10^{-3}\%
   \]
   and calculating the number of time constants
   \[
   e^{-t/\tau} = 5 \cdot 10^{-5}
   \]
   \[
   t \approx 10\tau
   \]

(d) Compare the slewing time to the settling time.
   **Solution:**
   - Negative slewing time: 2µs
   - Linear settling time: 1 \cdot 10^0 \mu s

9. **Topology Search**

Given the choice of NMOS or PMOS input stage, and the five different op-amp topologies that we have talked about (single-stage 5T diff pair with mirror load, single-stage current mirror, two-stage, telescopic cascode, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly ±0.6V, and that all overdrive voltages are roughly 0.1V.
(a) bandgap reference as in GLHM Figure 4.46c driving a 100kΩ load

Solution:
All structures could drive a 100kΩ load, as load resistance will not affect the DC gain too much.
In the bandgap, the input common-mode voltage is about 0.7V and the output voltage is around 1.2V.
NMOS input is the easiest choice. While a PMOS input might just work, the input common mode needed is close to the edge with $V_{dd} = 1.6V$.
With 0.1V over-drive voltage, all architectures could generate 1.2V output voltage (assume the cascode use high-swing current mirror load).

- Single-stage 5T diff pair with mirror load NMOS + PMOS
- Single-stage current mirror NMOS + PMOS
- Two-stage NMOS + PMOS
- Telescopic cascode NMOS + PMOS
- Folded-cascode NMOS + PMOS

Rubric: (10 Points)
• +1: Per correct topology choice
• -1: Per incorrect inclusion

(b) digital voltage regulator with an output of 1V and a supply of between 1.6V and 3.2V. Consider the scenarios with a load NMOS or PMOS device separately.

Solution:
For this LDO, with NMOS load, the minimum supply voltage is $1V + 2V_{ov} + V_{tn} = 1.8V$. This will not work with the low-end of the supply range.
With PMOS load, the input common voltage is 1V, and the output voltage is $V_{dd} - V_{ov} - V_{thp} = V_{dd} - 0.7V$. The PMOS input architectures would not work.

PMOS load:
- Single-stage 5T diff pair with mirror load NMOS
- Single-stage 5T current mirror NMOS
- Two-stage NMOS
- Telescopic cascode NMOS
- Folded-cascode NMOS

Rubric: (5 Points)
• +1: Per correct topology choice
• -1: Per incorrect inclusion

(c) analog voltage regulator with an output of 1.3V and a supply of between 1.6V and 3.2V.

Solution:
Similar as before, only NMOS input architectures work.

PMOS load:
• Single-stage 5T diff pair with mirror load NMOS
• Single-stage 5T current mirror NMOS
• Two-stage NMOS
• Telescopic cascode NMOS (just work)
• Folded-cascode NMOS

Rubric: (5 Points)
• +1: Per correct topology choice
• -1: Per incorrect inclusion

(d) ADC comparator with an input at 1.25V and a supply at 1.25V.
Solution:
Must use an NMOS input folded cascode, as those are the only ones where the input common mode includes the top rail.

• Folded cascode NMOS

Rubric: (1 Points)
• +1: Per correct topology choice
• -1: Per incorrect inclusion

(e) variable gain amplifier with an input at 0V and a supply at 1.25V.
Solution:
Must use a PMOS input amplifier to include the bottom rail in the input common mode range.

• Folded cascode PMOS

Rubric: (1 Points)
• +1: Per correct topology choice
• -1: Per incorrect inclusion

10. PMOS Input Folded Cascode
For the PMOS-input folded cascode op-amp below, assume the quadratic model with the following process specs:

\[
\begin{align*}
\mu_n C_{ox} & = 2 \mu_p C_{ox} = 200 \mu A/V^2 \\
\lambda & = 0.1 V^{-1} \\
V_{in} & = -V_{tp} = 0.3 V \\
V_{DD} & = 2 V \\
C_{ox} & = 5 \text{ fF/um} \\
C_{ol} & = 0.5 \text{ fF/um}
\end{align*}
\]
(a) Calculate and tabulate:

i. the overdrive voltage and current in all devices. For this step you may assume that \( \lambda = 0 \). The simplest order may be \( Mb1 \) through \( Mb6 \), then \( M1 \) through \( M5 \).

Solution:
We’ll start with \( Mb1 \) and work our way through devices

\[
I_{D,b1} = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} V_{ov}^2
\]

\[
100 = \frac{1}{2} \times 200 \times \frac{100}{1} \times V_{ov}^2
\]

\[
V_{ov,b1} = 0.1 \text{V}
\]

Note that \( Mb5 \) is \( \frac{10}{1} \)—a factor of 10 smaller than the other devices! For the same current, it needs an overdrive \( \sqrt{10} \times \) larger than its \( \frac{100}{1} \) brethren.
### ii. Calculate the bias voltages on all nodes, assuming $V_{in,CM} = 1V$. Specifically: tail, G2, G3, G5, Gb6, S3B, S4AB, and out.

**Solution:**
This one is really a lot of $V_{GS} = V_t + V_{ov}$ (for the NMOS—switch signs for PMOS).

<table>
<thead>
<tr>
<th>Node</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tail</td>
<td>1.4</td>
</tr>
<tr>
<td>G2</td>
<td>0.4</td>
</tr>
<tr>
<td>G3</td>
<td>0.62</td>
</tr>
<tr>
<td>G5</td>
<td>1.6</td>
</tr>
<tr>
<td>Gb6</td>
<td>1.6</td>
</tr>
<tr>
<td>S3B</td>
<td>0.22</td>
</tr>
<tr>
<td>S4A/B</td>
<td>1.6</td>
</tr>
<tr>
<td>out</td>
<td>1.2</td>
</tr>
</tbody>
</table>

### iii. the $g_m$ and $r_o$ parameters for M1 through M5.

**Solution:**
Assuming our devices are in saturation,

$$g_m = \frac{2I_D}{V_{ov}}$$

$$r_o = \frac{1}{\lambda I_D}$$

<table>
<thead>
<tr>
<th>Device</th>
<th>$g_m$ (mS)</th>
<th>$r_o$ (MΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>2</td>
<td>0.1</td>
</tr>
<tr>
<td>M2</td>
<td>4</td>
<td>0.05</td>
</tr>
<tr>
<td>M3</td>
<td>2</td>
<td>0.1</td>
</tr>
<tr>
<td>M4</td>
<td>2</td>
<td>0.1</td>
</tr>
<tr>
<td>M5</td>
<td>2</td>
<td>0.1</td>
</tr>
</tbody>
</table>

**Rubric:** (40 Points)
(b) Calculate $G_m$, $R_o$, and $A_{v0}$

**Solution:**

\[
G_m \approx g_{m1} \\
R_o = R_{o, up} || R_{o, down} \\
\approx (g_{m4} r_{o5} r_{o4}) || (g_{m3} r_{o3} (r_{o2} || r_{o1})) \\
= (20 \text{M}\Omega) || (6.67 \text{M}\Omega)
\]

\[
|A_{v0}| = G_m R_o
\]

\[
G_m = 2 \text{mS} \\
R_o = 5 \text{M}\Omega \\
|A_{v0}| = 10,000 \text{V}
\]

**Rubric:** (3 Points)

• +1: Per correct answer

(c) Calculate the input common mode range and output swing.

**Solution:** Calculating the input common mode range:

\[
V_{iCM, max} = V_{DD} - V_{ov5} - V_{SG1} = 1.5 \text{V} \\
V_{iCM, min} = V_S3 - V_t = -0.08 \text{V}
\]

Calculating the output swing:

\[
V_{out, max} = V_{DD} - V_{SG5} - V_{ov4} = 1.5 \text{V} \\
V_{out, min} = V_G3 - V_t = 0.32 \text{V}
\]

\[
V_{iCM} \in [-0.08, 1.5] \text{V} \\
V_{out} \in [0.32, 1.5] \text{V}
\]

**Rubric:** (8 Points)
(d) What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing? How would you change the size of Mb5 to achieve that voltage?

Solution:

\[ V_{G3,\text{min}} = V_{ov2} + V_{GS3} = 0.5V \]

For the common mode range and swing:

\[ V_{iCM,\text{max}} = V_{DD} - V_{ov5} - V_{SG1} = 1.5V \text{ (no change)} \]
\[ V_{out,\text{max}} = V_{DD} - V_{SG5} - V_{ov4} = 1.5V \text{ (no change)} \]
\[ V_{iCM,\text{min}} = V_{S3} - V_{t} = V_{G3} - V_{GS3} - V_{t} = -0.2V \]
\[ V_{out,\text{min}} = V_{G3} - V_{t} = 0.2V \]

And finally to change the sizing of Mb5 to get that voltage:

\[ V_{ovb5} = V_{G3} - V_{t} = 0.2V \]
\[ I_{Db5} = \frac{1}{2} \mu_n C_{ox} W \frac{V_{ovb5}^2}{L} \]
\[ W = \frac{2 I_{Db5}}{\mu_n C_{ox} V_{ovb5}^2} \]
\[ \frac{W}{L} = 25 \]

which makes sense since to sink the same current with twice the overdrive requires a size down of 4× relative to the larger device.

\[ V_{G3,\text{min}} = 0.5V \]
\[ V_{iCM} \in [-0.2, 1.5] V \]
\[ V_{out} \in [0.2, 1.5V] V \]
\[ \left( \frac{W}{L} \right)_{b5} = 25 \]

Rubric: (7 Points)
- +1: Correct method for \( V_{G3,\text{min}} \)
- +1: Correct numerical value for \( V_{G3,\text{min}} \)
(e) If the load capacitance is roughly 1pF (roughly the same as the input capacitance),

i. what are the pole and unity gain frequencies?

**Solution:**

We have a dominant pole

\[
\omega_p = \frac{1}{R_o C_L} = \frac{1}{5 \text{M}\Omega \times 1 \text{pF}} = 0.2 \times 10^6 \text{rad/s}
\]

\[
\omega_u = \frac{G_m}{C_L} = \frac{2 \text{mS}}{1 \text{pF}} = 2,000 \times 10^6 \text{rad/s}
\]

Rubric: (2 Points)

• +1: Correct \(\omega_p\)
• +1: Correct \(\omega_u\)

ii. what is the phase margin in unity gain?

**Solution:**

To calculate the phase margin we should first calculate non-dominant poles and zeros. The two diode connections give 2 poles and a zero while the cascode contributes one non-dominant pole. The respective values are as shown:

\[
\omega_{p, \text{cascode}} = \frac{g_{m3}}{C_{gs,3}} = \frac{g_{m3}}{\frac{2}{7} W_3 L_3 C_{ox} + W_3 C_{ol}}
\]

\[
= \frac{g_{m3}}{2,000 \mu\text{S}}
\]

\[
= \frac{5.22 \times 10^8 \text{rad/s}}{2,000 \mu\text{S}}
\]
ω_{p,\text{mirror}1,2} = \frac{g_{m5}}{2C_{g_{\text{s,5}}}}
= 1.3 \times 10^9 \frac{\text{rad}}{\text{s}}

ω_{c,\text{mirror}} = \frac{g_{m5}}{\sqrt{2}C_{g_{\text{s,5}}}}
= 1.84 \times 10^9 \frac{\text{rad}}{\text{s}}

Calculating the phase margin can be found as

\phi_{PM} = 180 - \tan^{-1}\left(\frac{\omega_u}{\omega_p}\right) - 2\tan^{-1}\left(\frac{\omega_u}{\omega_{p,\text{mirror}}}\right) + \tan^{-1}\left(\frac{\omega_u}{\omega_{c,\text{mirror}}}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p,\text{cascode}}}\right)

\approx -8^\circ

using the small angle approximation.

\phi_{PM} \approx -8^\circ

Rubric: (7 Points)
• +1: Per correct method for calculating a non-dominant pole or zero (4x)
• +5: Correct method for calculating phase margin
• +1: Correct numerical value of phase margin

iii. what are the frequencies of the pole/zero doublets from the current mirror?

Solution:
See above.

Rubric: (2 Points)
• +1: Per correct answer

11. Continuing...

To increase the positive output swing of the previous amplifier,

(a) redraw the PMOS current mirror M4AB, M5AB as a high-swing cascode current mirror, as in Figure 5.18b in Razavi (5.13b in the 1st edition), but PMOS.

Solution:

![Diagram of PMOS current mirror and cascode configuration]
This presents a couple of issues:

- What is the “right” value of $V_{BP}$ (especially across supply and temperature)
- How to generate $V_{BP}$?

**Rubric:** (1 Points)
- +1: Correctly redrew the figure as PMOS

(b) Generate $V_b$ ($V_{G4}$) using something like Mb5 above, but PMOS. What current source do you use? What gate voltage biases it? What ($\frac{W}{L}$) do you use for all devices, and why?

**Solution:** There are a few different ways to achieve this. The first way is generating $V_{BP}$ independent of the actual mirror with something like so:

$$V_{BP} = V_{DD} - V_{SG,Mb}$$

$$= V_{DD} - \left( \frac{2I_D}{\mu p C_{ox} \frac{W}{L} + V_{tp}} \right)$$

$$= V_{DD} - (2V_{ov} + V_I)$$

$$\left( \frac{W}{L} \right)_{Mb} = \frac{1}{4} \times \left( \frac{W}{L} \right)_4$$

Alternatively, you can resort to what’s known as the self-biased mirror:
where

\[ V_{\text{bot}} = V_{\text{SGAB}} + V_{\text{ov}} \]
\[ = V_{\text{top}} + I_{\text{REF}} R_b \]

To have the same \( I_{\text{REF}} = I_O \), \( M4A = M4B = M5A = M5B \), so

\[ V_{\text{SGAB}} = V_{\text{SG5A}} = V_{\text{top}} \]

and so to remain in saturation,

\[ R_b \leq \frac{V_{\text{ov}}}{I_{\text{REF}}} \]

**Rubric:** (4 Points)
- +1: Some viable circuit
- +3: Indication of restrictions associated with the biasing circuit (e.g. current sources, gate voltage, device sizing)

(c) **(EE240A)** Generate \( V_b \) from the circuit suggested in 5.19b in Razavi. What value for \( \left( \frac{W}{L} \right)_5 \) in that figure is needed?

**Solution:**
For reference, the topology:
We know $V_{\text{OUT}} = 1.2\text{V}$, meaning $V_{ov5} = 0.5\text{V}$. To sink the same amount of current as in the previous subparts, we consider the ratio of the new $V_{ov}$ and the old one. If it increases by a factor of 5, the size needs to decrease by a factor of 25 to sink the same amount of current as before, so

$$\left(\frac{W}{L}\right)_5 = \frac{8}{1}$$

**Rubric:** (2 Points)
- +2: Correctly solved for $\left(\frac{W}{L}\right)_5$