EECS140 Midterm 1
Spring 2017

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SID_____

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1. [4] A single-pole amplifier has a low frequency gain magnitude of 500 and a gain magnitude of 5 at 1 GHz. What are the pole and unity gain frequencies?

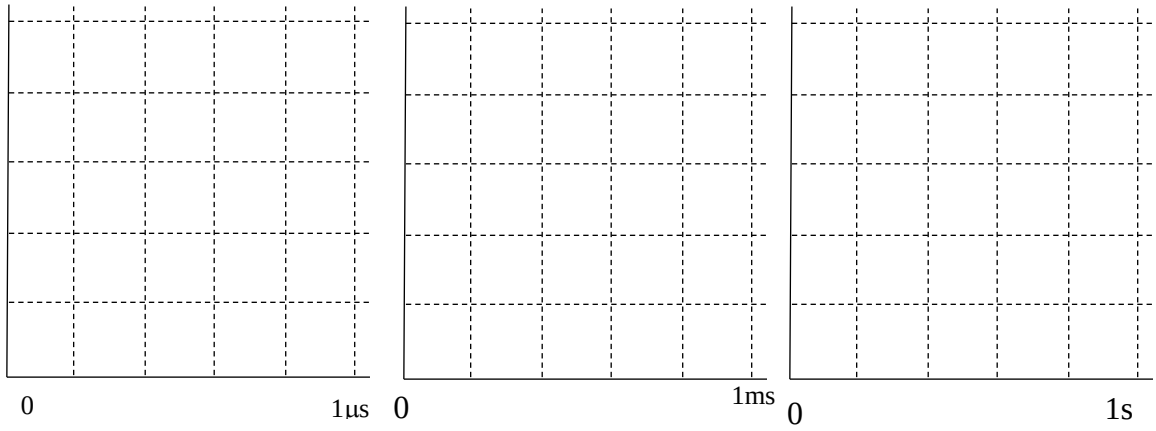
2. [8] You have made a new NMOS transistor. You measure the drain current as a function of the gate-to-source and drain-to-source voltage, and find that it is $I_d = \alpha(V_{gs}-1V)^{1.5}(V_{ds})$ when $1V<V_{gs}<10V$ and $0<V_{ds}<10$, where α is a positive constant with appropriate units.
    a. Write an expression for the transconductance in terms of just voltages, and in terms of I_d and some voltages.

    b. Write an expression for the output resistance in terms of I_d

    c. Write an expression for the intrinsic gain in terms of the bias point

    d. To maximize the gain, where would you bias this device (what voltages)?

3. [5] A voltage source with a 1MΩ output impedance drives an amplifier with a 1nF input capacitance. At t=0, the voltage source jumps from 0 to 1V (a step input). Carefully sketch by hand the voltage seen at the input to the amplifier on three different time scales:
    a. 0 to 1 μs
    b. 0 to 1 ms
    c. 0 to 1 s



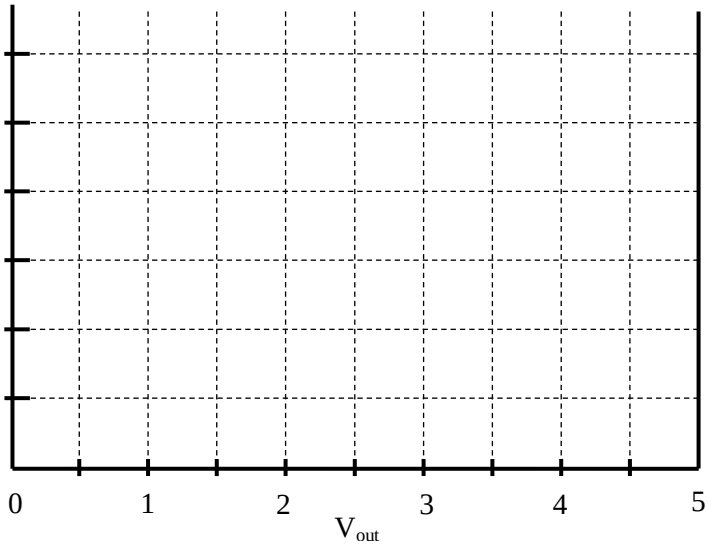
4. [5] By hand, sketch the response of the RC filter above to an input sine wave with a 1V amplitude and a frequency of 1,000 rad/s. Draw the input for reference, and then the output. Label both axes. Label the input and output sine waves.

5. [8] You have an NMOS-input common source amplifier with a PMOS load and a large load capacitance. Both transistors are biased in saturation, and the quadratic model is appropriate. The magnitude of the gain is large (>100). You try two independent changes to the circuit. Case 1: doubling the width of both devices. Case 2: doubling both the width and the length of both transistors without changing anything else. How do these changes affect the operating point and performance of the amplifier?

Process specs $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda=1/(10V)(L_{min}/L)$, $-V_{tp}=V_{tn}=1V$, $V_{DD}=5V$, $L_{min}=1um$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5$ fF/um.

	I_D	V_{ov}	g_m	R_o	Av	ω_p	ω_u	C_{in}
Case 1								
Case 2								

6. [12] In the same process described above, you have made a similar amplifier with $(W/L)_N=10u/1u$, $(W/L)_P=20u/1u$. You choose $V_{GSN}=1.2V$.
   a. [4] Carefully sketch I_{DN} vs. V_{out}. Put a dot at the transition between triode and saturation. Get the slope right in saturation.
   b. [2] What input voltage V_{Pmid} will result in an output voltage of 2.5V?
   c. [2] Sketch the magnitude of the PMOS current vs. V_{out} if the input is held at V_{Pmid}.
   d. [4] What is the output swing?



7. [12] Fill in the following table for a single-pole amplifier. Each row is a different amplifier.

g_m	R_o	C_L	A_{v0}	ω_p	ω_u
		1uF	1000		10 M rad/s
		1nF	10^6	10 rad/s	

8. [6] Here's a power MOSFET made at Virginia Tech. The vertical axis is in Amps, from 0 to 12. The horizontal axis is in Volts, from 0 to 12.
   a. What is a rough guess at the threshold voltage?

   b. Roughly what is g_m when $V_{GS}=V_{DS}=7V$?

   c. Roughly what is r_o when $V_{GS}=V_{DS}=7V$?