Proj & Report #2 M/Tu

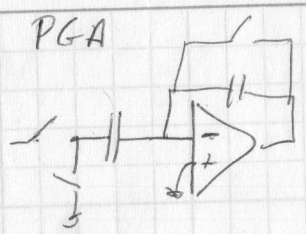
should have some full system integration results

PGA correction

rail-to-rail in/out

Regulators

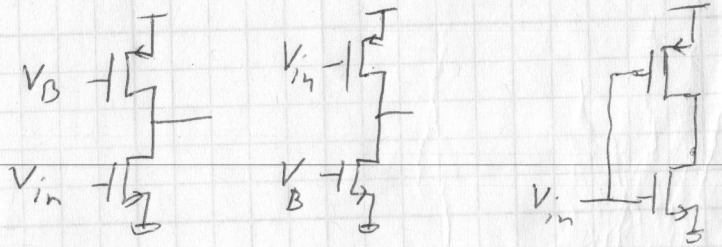
PGA

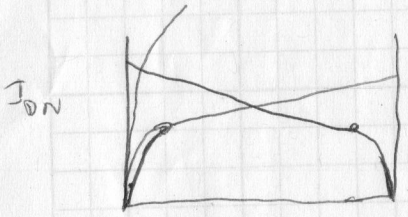


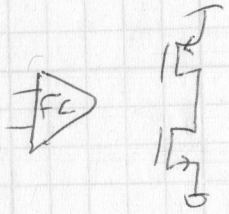
need to drive PGA output to 0

⇒ 2nd stage

NMOS CS, or PMOS? or both?







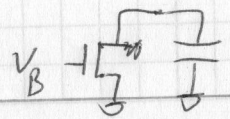
Driving NMOS: big increase in I_{on}

pulls output down fast (good)

but never gets to 0.

Driving PMOS: decrease in $|I_{dp}|$ (to 0)

⇒ and it's the same RC as a switch



Debugging

1) modularity, source code control

if it works, name it, copy it
re-use it, but don't touch it

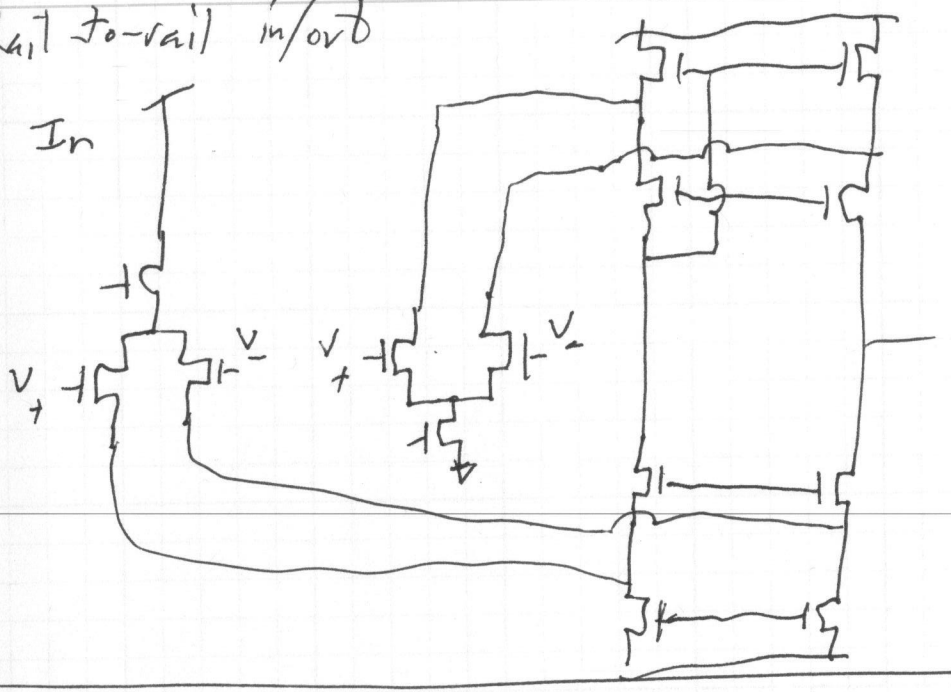
2) Don't hack. Simplify until you understand, then build back up.
use piazza, OH

3) start w/ supply, bias voltages, branch currents.
Ideal sources, simple feedback
ideal feedback, etc.

make sure that you understand before you move on

140/240A 17 SP W13L3

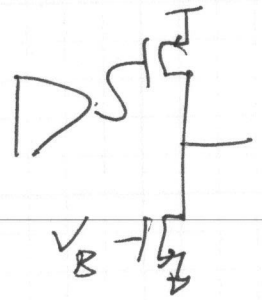
OPA 340
Rail-to-rail in/out



- need to be careful of tail current biases
- Actually V_{iL} goes beyond both rails

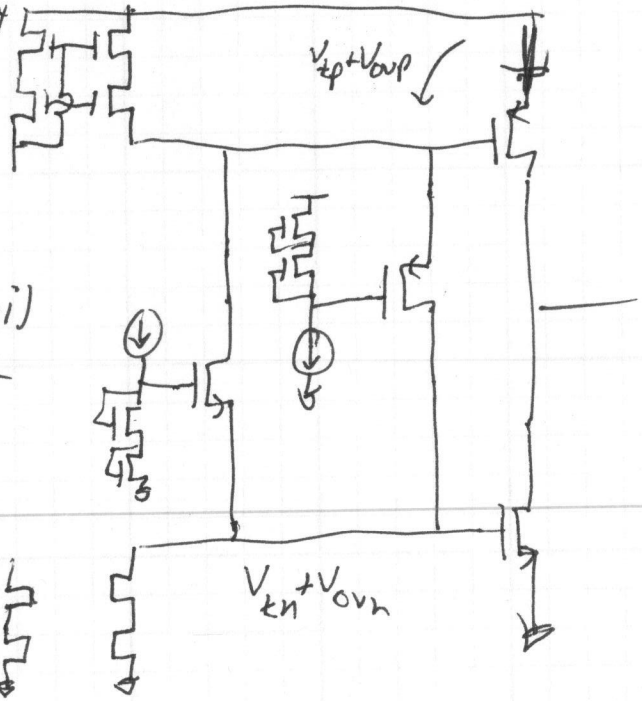
OVT

PGA



Can drive:
Capacitive load to 0 but not V_{DD}
Resistive load close to V_{DD}, but not 0

OPA family



- gain boost
- Rail-to-rail input OK

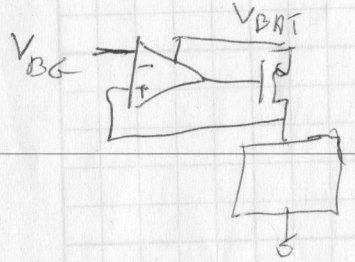
Regulators

Varying digital current is the main problem

Varying Temp, V_{BAT}

Last time I_{DD} ↑ ↓ $Q_{pulse} \simeq 0.16\,nC$ → t

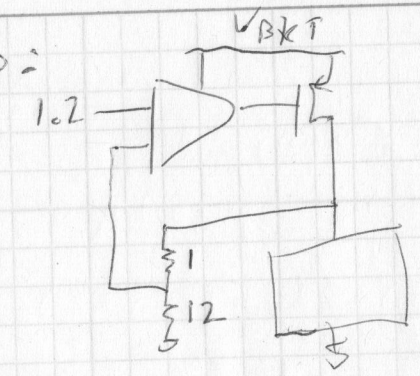
$\Rightarrow \Delta V_{cap} = 0.16V$



1) reduce magnitude of voltage change

2) shift it up a bit

shift it up:



reduce magnitude

→ need voltage gain around the loop at 10MHz

already have gain around the loop at low frequency. Must be > 10 to meet spec.

At 10MHz $|Z_{cap}| = \frac{1}{\omega C} = \frac{1}{(2\pi \times 10^7)(10^{-9})}$

$= \frac{100}{2\pi} \simeq 16$

2nd stage gain = ?

$\omega_{p2} = \frac{1}{R_0 C_L}$

$R_0 = r_{op} \| r_{odigital}$

$\frac{1}{\lambda I_D}$ ↑

$\omega_{p2} < \frac{1}{r_{o2} C_L} = \frac{\lambda I_D}{10^{-9}} = 10^9 [0.1, 1] \{1, 5\}$ m

$= 10^6 [0.1 - 5]$

$f_{p2} = 10^4 - 10^6$ MHz

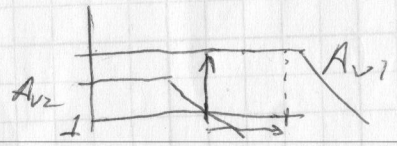
So at 10 MHz, g_{m2} is driving the cap.

@ 10 MHz

$|A_{V2}| = \frac{g_{m2}}{\omega C_L} = \frac{2I_D}{V_{ov}}$ (16 Ω)

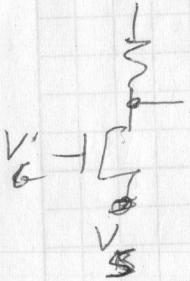
$g_{m2} = \frac{2\{1,5\}mA}{[0.1-0.3]} = [6-100]\,mS$

$A_{V2}(10\,MHz) \simeq [0.1-2]$



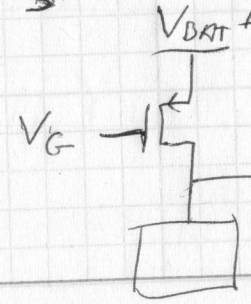
need $\omega_{p1} > |A_{V1,0}|\,\omega_{u2} = \omega_u$ for stability

problem? Consider



$A_{G\to D} = -g_m R_D$

$A_{S\to D} = g_m R_D$



if V_G = const

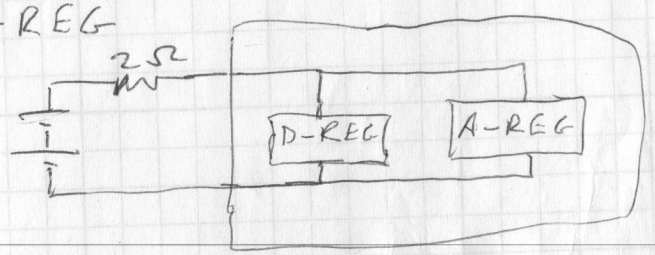
$\frac{v_{dda}}{v_b} = g_m R_D$

$v_b = 8mV$ @ 10 MHz

also need

$|A_{V1,0}|\,A_{V2}(j2\pi 10^7)$ big enough to knock down ripple e.g. >10

A-REG

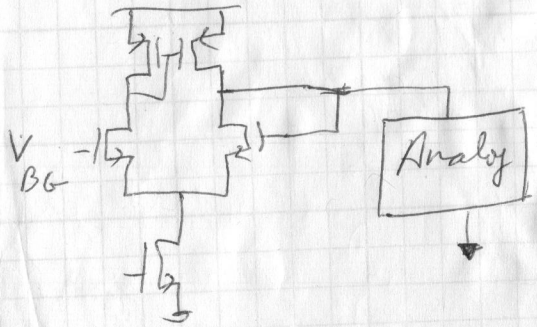


with no ripple on V_{DDD} with each digital pulse, on-chip V_{BAT} drops (2Ω)(4mA) = 8mV

So don't make V_G const @ 10 MHz

i.e. make sure that there is gain.

Do you need 2 stage?



why not do this? With digital too?