Corrections
leakage < 1pA ⇒ wrong. Often Lisler.

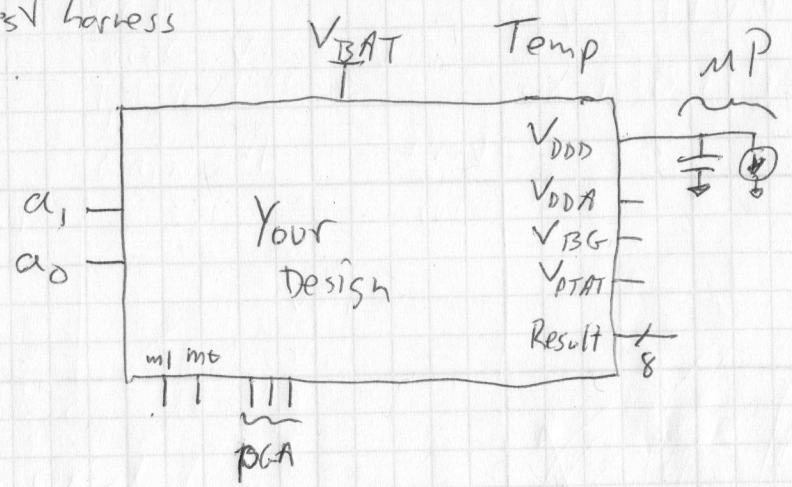
You don't know enough to design ⇒ true in general
but you do know enough to
meet the project specs

test harness

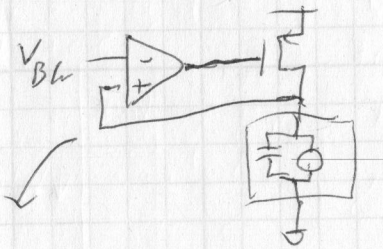
charge injection

regulators

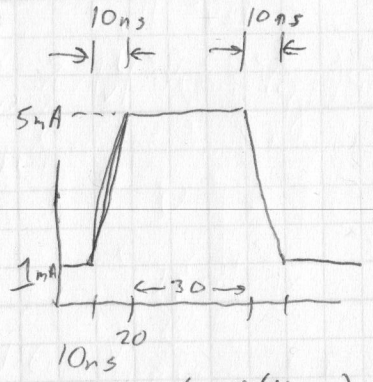
test harness




Regulators




or




charge in each spike = (4mA)(40ns)

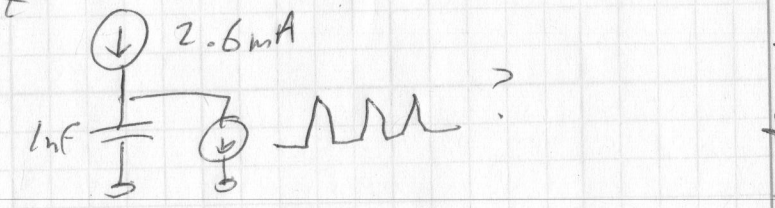
= 160pC = 0.16nC

$\frac{0.16nC}{100ns} = 1.6mA$

average current: 2.6 mA

$260\frac{\mu A}{MHz}$ ≈ typical 32 bit µP

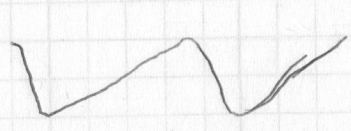
what if




$\Delta Q = 0.16nC$ $\Delta V = \frac{\Delta Q}{C} = \frac{0.16nC}{1nF}$

$= 160mV$

If you center the 10 MHz dips, it meets the spec!




0.16 V = ± 80mV < ±10%

Debugging

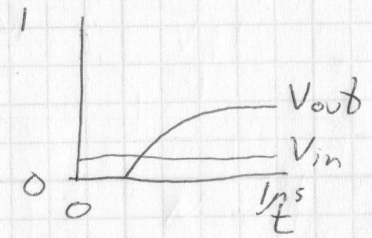
Presenting results

- make it clear what you are talking about
  - what circuit - ADC w/ ideal input voltage and supply
  - what test conditions — 25C, $V_{DDD}$=1.2V, $V_{ref}$=1.0V
  - what expected result

should see $b_7$ $b_6$ $b_5$ so 1.0V, 3.0V, instead

explain what it means "because there is charge leaking..."

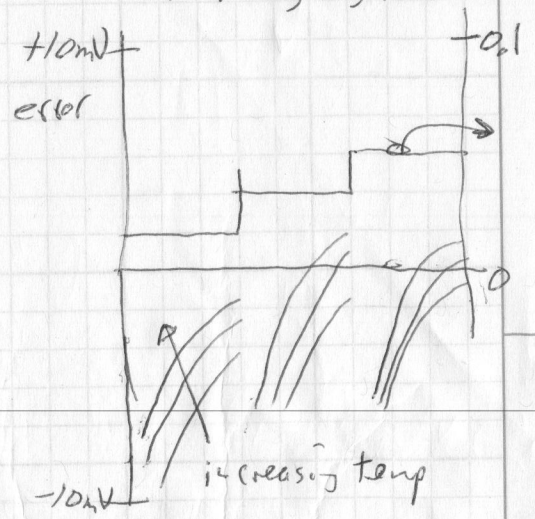
PGA
70C, $V_{BAT}$=3.6V
1pf load
GAIN = 4




OK, but

can't see the error. 4mV? 10mV?

$V_{BAT}$ = 1.6, 2.4, 3.6V
or T = 0, 25, 70°C




PGA
ideal supply
worst error

| Temp \ $V_{BAT}$ | 1.6 | 2.4 | 3.2 |
|---|---|---|---|
| 70 | | | 70mV |
| 25 | | 1mV | |
| 0 | | | |

$V_{BAT}$

Full system
LSB error
temp conversion

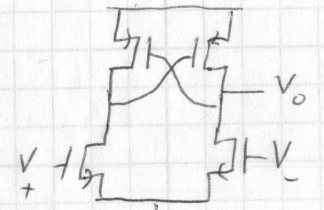
| Temp \ $V_{BAT}$ | 1.6 | 2.4 | 3.2 |
|---|---|---|---|
| 70 | 3 | 7 | |
| 25 | 0 | 5 | |
| 0 | 42 | | |

$V_{BAT}$

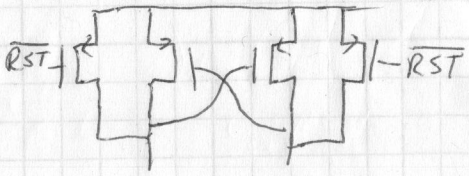
Comparator

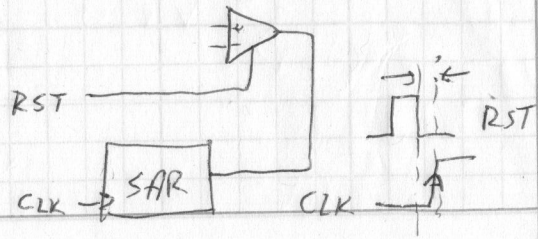
1) use thick ox (high $V_t$) input devices

2) use caution w/ strong arm



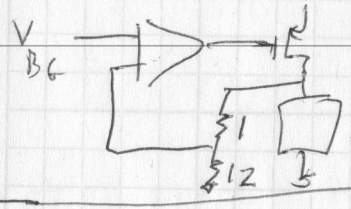

simplified version




does not meet spec.

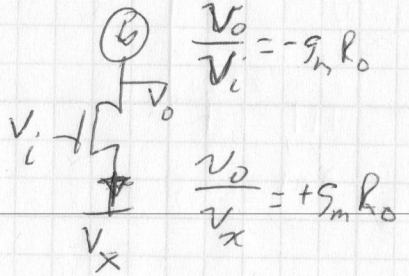

does meet spec

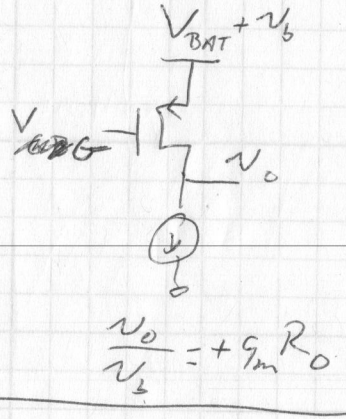



What about supply variation?

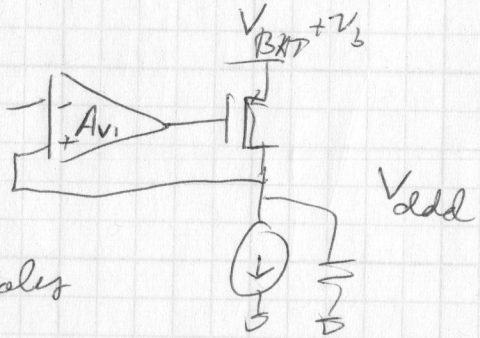
DC, AC

First, consider:

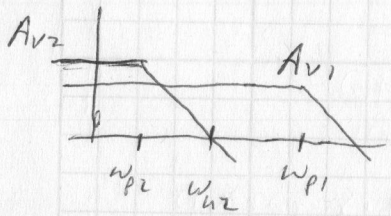


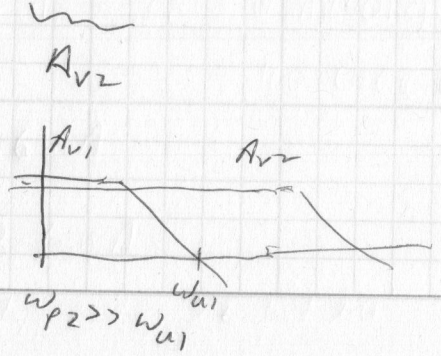

In feedback




For stability need poles separated, either




or




$\omega_{p1}$ much higher than $\omega_{u2}$

For digital reg, pretty clear. Output cap is huge, make $\omega_{p2}$ dominant, make 1st stage any low gain and fast. (short channels)

For analog regulator, if $\omega_{p1} << \omega_{p2}$ then at 10 MHz, $V_{dd} \approx 0$