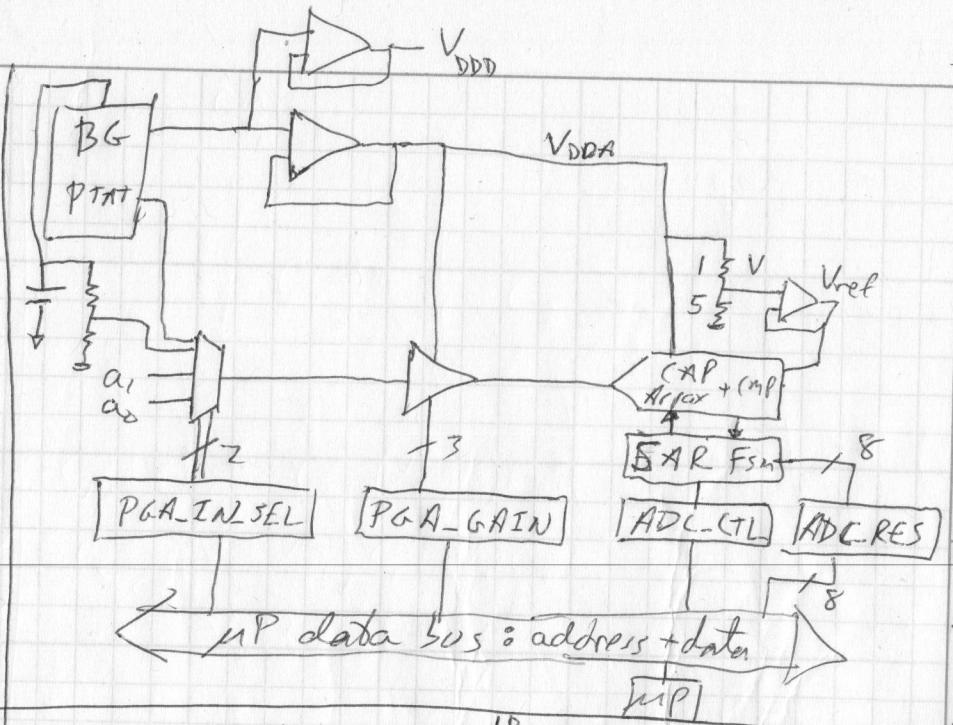
Presentations – Have ppt ready to go

Design Due < 2 weeks!

- integration!

System block diagram, ADC/PGA timing

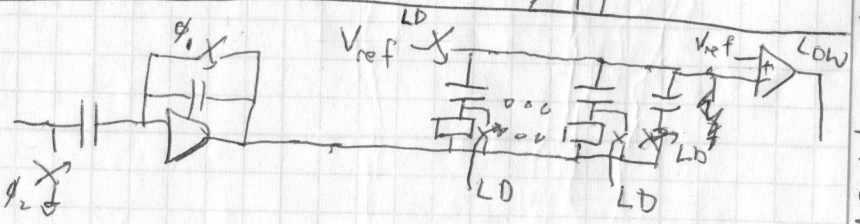
Switches, take 2



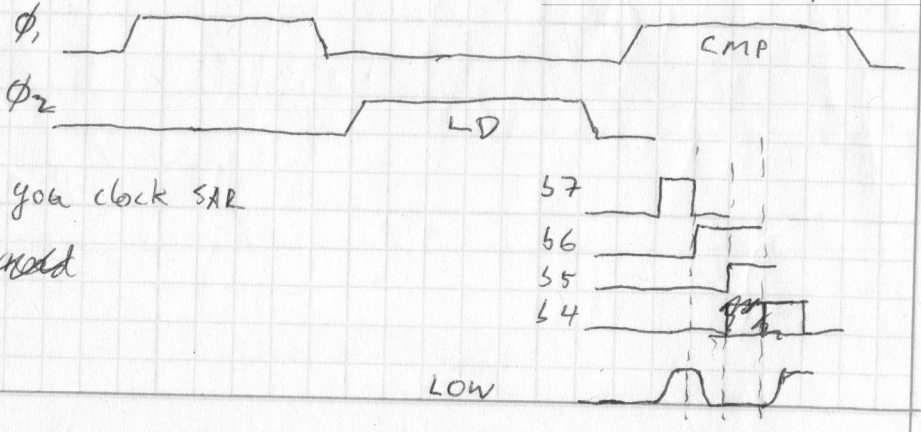
example embedded code

```
#include "analog.h"
PGA_IN_SEL = PTAT ; #defined values elsewhere
PGA_GAIN = 1;
ADC_SAMPLE();
for(i=0; i<100; i++) ; delay to let ADC cycle
x = ADC_RES;
```

typically these are all memory mapped registers



many timing options. One simple one: let LD = ϕ_2



you clock SAR

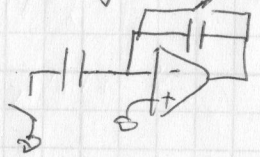
could

You get to decide ϕ_1, ϕ_2 and pick a digital clock frequency

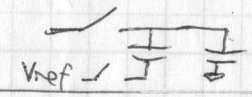
Some issues w/ switches

- fwd bias junctions

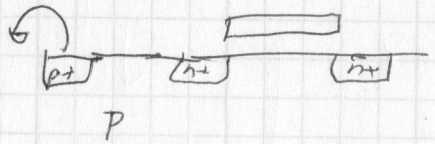
PCA

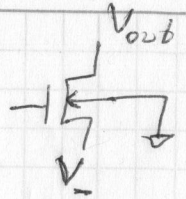


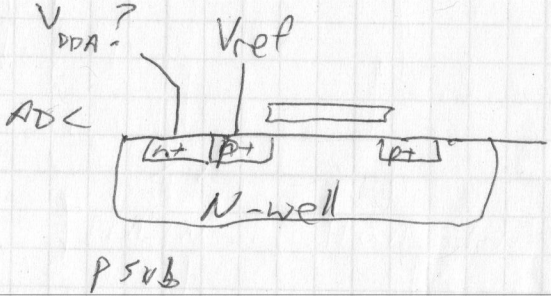
ADC

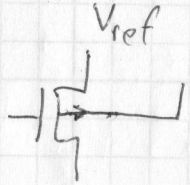


PCA:



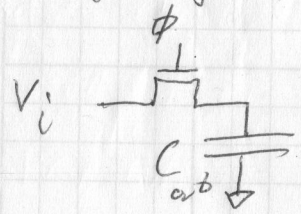




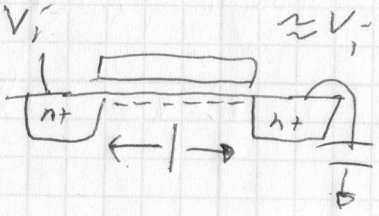


$(V_{ref} - V_{in}) + \frac{1}{2} V_{ref}$

Charge injection



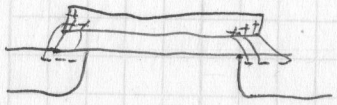
after settling

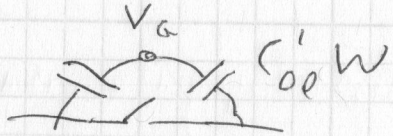


in the linear region $C_{gs} = \frac{1}{2} WL C_{ox} + C'_{ol} W$

$C_{gd} = \frac{1}{2} WL C_{ox} + C'_{ol} W$

$V_{GS} = V_{th}$





say $W = 1\mu m$ $C'_{ol} = 1 fF/\mu m \Rightarrow C_{gd} = 1 fF$

$V_{th} = 0.2V$

$Q = (V_{th})(C_{gd}) = 0.2 fC$

$\Delta V_{\text{charge injection}} = \frac{Q}{C_{out}} = \frac{V_{th} C_{gd}}{C_{out}}$

$= 0.2V \frac{1 fF}{C_{out}}$

$C_{out} = 1pf \Rightarrow 0.2mV$

$C_{out} = 4ff \Rightarrow 50mV$