FINAL DESIGN due Monday, 5/1/2017 9am


1→ 1.2

no layout? XC?

Golden Bear Circuits is working on its next exciting circuit product. This is a mixed-signal chip for embedded "Internet of Things" applications, with a microprocessor, flash and RAM memory, and a handful of analog inputs and outputs. You are a part of the three-person analog design team, and need to design all of the analog components for this chip. This includes:

- 8 bit successive-approximation analog to digital converter (ADC)

- programmable gain switched capacitor pre-amplifier (PGA)

- Bandgap voltage reference and Temperature sensor (BGT)

- Analog multiplexer (MUX)

- Analog and digital voltage regulators (REGs)

The digital team is handling the two Pulse Width Modulation (PWM) DACs.
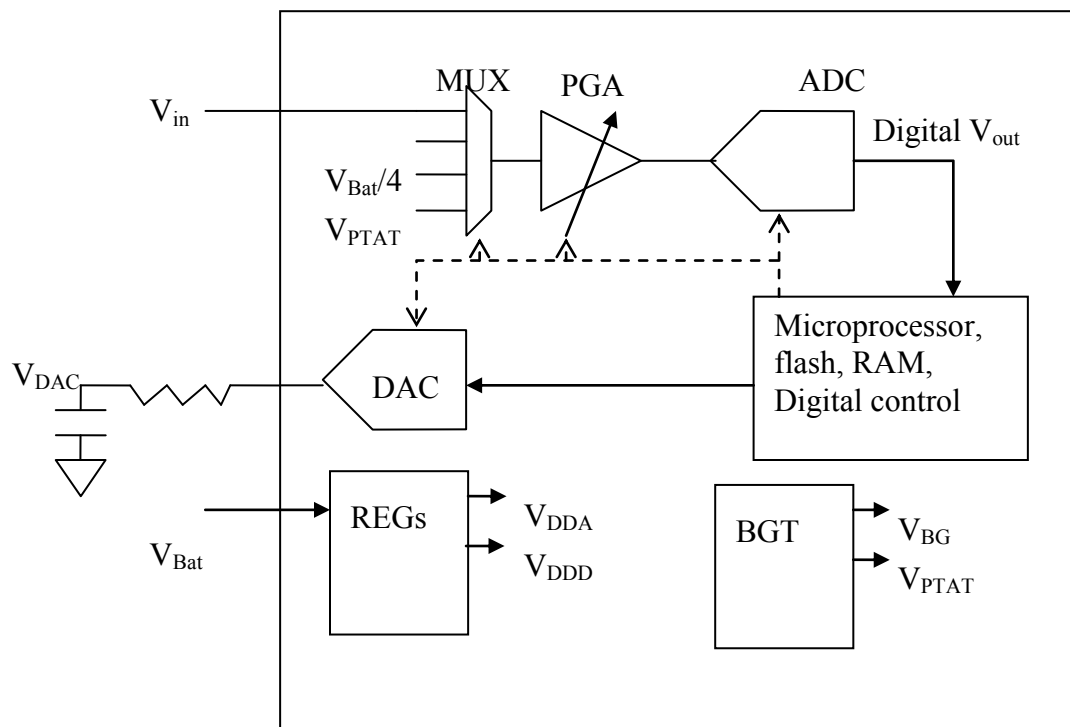
The product will be battery powered, so the circuits need to operate properly from as high as 3.2V (two brand new alkaline batteries) down to 1.6V or less (two alkaline batteries at end of life). Assume that each battery has 1Ω series resistance, or 2Ω total. The product will be used in consumer electronics, so all specs must be met over the range from 0 to +70 Centigrade. All of the circuit blocks share a common ground. The microprocessor is the only block that runs off of V_{DDD}. All other blocks run off of either V_{DDA} or V_{BAT}. V_{DDD} should be nominally 1.2V, and V_{DDA} should be the output of your bandgap reference.

ADC – Analog to Digital Converter

The ADC must use an 8 bit successive approximation charge-redistribution topology [1]. The digital output of the ADC taken as an integer between 0 and 255, times 1V/256, should be within 1 LSB of the analog input being sampled. In other words, each LSB should be just under 4mV. The digital SAR circuitry will be supplied to you by the digital team. We need to be able to take at least 100k samples/second.

PGA – Programmable Gain Amplifier

The programmable gain amplifier must have a gain of all integers between 1 and 8 inclusive, implemented with switched capacitors. The gain error must be less than 0.4% (which is 1 LSB of the ADC) for all gain settings. The gain setting is controlled by digital signals from the microprocessor.

BGT - Bandgap and Temperature sensor

The bandgap reference must be accurate to within 5mV after digital trim. Each LSB of a converted temperature measurement must correspond to 2 Kelvin, e.g. room temperature should give ADC readings of around 145 to 150.

MUX – Analog Multiplexer

The analog MUX must allow the microprocessor to select from one of 2 external analog inputs, as well as measure the battery voltage and the current temperature of the chip. The mux is controlled by digital signals from the microprocessor.

REGs

The regulators must take the battery voltage and deliver a clean supply to the analog and digital blocks. The digital block runs at 10MHz and pulls a peak current of 5mA, and its supply must stay within 10% of $V_{DDD,nom}$. The digital circuits present a periodic load which we model as a constant 1nF capacitance in parallel with a constant 1mA current and a periodic 4mA current. For example:

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Iddd          ddd    0      pulse (1m 5m 10n 10n 10n 30n 100n )

Cdigital      ddd    0      1n
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The analog blocks you design yourself, so you decide what they need. The DAC will pull up to 100uA from V_{BG}, which should probably have a separate output buffer for the DAC.

Design restrictions

- Your circuit can contain as many MOSFETs and capacitors as you wish. MOSFET dimensions should be in multiples of 0.1um. The smallest MOSFET allowed is W/L=0.2u/0.1u. Capacitors used in any feedback network must have an integer ratio (e.g. C1=C2, or C1=16*C2). For example, C1=15.8*C2 is explicitly not allowed.

- Your circuit may contain resistors, but you must lay them out and extract them, because most have weird nonlinearities and temperature dependence.

- Your circuit may contain off-chip passives (e.g. a big capacitor).

- The minimum sized capacitor that can be made reliably is 4fF.

- Other than the control signals that come out of the digital SAR block, you may have two ideal non-overlapping clocks, with rise and fall times no shorter than 5% of the overall period.

- We're using an NWELL CMOS process for this run, so all NMOS devices share a common bulk terminal.

This is a group project. Your team of three will all be evaluated together.

Presentations

Your whole team will do three formal presentations, two to me, and one to the whole class.

In the first meeting, I'd like you to present your planned schedule and division of labor: who will do what by when. You should have a block diagram of the project, with some detail on what kinds of amplifiers and other circuits will be needed in each block. You will also need to give me a list of how responsibility will be divided among each of you for each of the five components of the project. Everyone on the team must have at least 10% responsibility for every component. Your end-of-the-year bonus will depend on how your parts of the project turn out (think of it like a grade!). If you would like to propose how your bonus should be calculated, in terms of how much credit you get for meeting performance and schedule milestones, this is the meeting in which to do so.

In the second meeting, I'd like to have a design review where you present your preliminary results. These should be fairly complete implementations of all of the blocks

using semi-ideal amplifiers and switches. In this meeting you should also discuss what tests you're planning to run on each block.

Your final presentation will be in class during RRR week. You will have 15 minutes to summarize the performance of your design, but the presentation should include all of the backup information necessary to explain in detail all of your design decisions and performance. Examples of things to include:

- Enumeration of the constraints and specs for each block, and how these led to the choice of amplifier/circuit topology, as well as gain, bandwidth, input common mode range, output swing, operating points, etc.

- Failures that resulted in changes in the design

- Hand calculations of performance vs. simulation results for all blocks

- Simulated performance of each block over the voltage and temperature range, compared to specs. This should include the performance of the block by itself with an ideal supply, as well as the operation of the block with as much of the whole system running as possible. Specifically, showing that your block works with the regulators on and the "microprocessor" running. This is the most important part of the presentation, and these simulations will take you longer than the design itself.

- Design area and cost. For MOSFETs, use 10WL. Resistors must be laid out and extracted. Capacitors are $1fF/\mu m^2$. For external passives use digikey to get cost, and add $200\mu m^2$ die area per i/o pin to account for bond pad area. Assume overall CMOS cost is $0.10/mm^2$.

- Each member of the 240A group must have at least one op-amp laid out and extracted, and compare performance with hand calcs and schematic simulation.

The presentation is a good place to create documentation as you go along. The block diagram that you show me in the first meeting is likely to be in your final presentation as well.

Your design coach (Brad) will be available in the lab each week, for brainstorming and design reviews. I'm happy to have more than two meetings as well, but I'd like to have the entire team present, and an updated presentation, for any meeting that we have.

Performance Metrics

A small number of additional points will be awarded to the teams with

- the lowest power consumption

- the lowest cost (which is smallest die area if there are no externals)

- the lowest battery voltage for which all specs are met

If you're looking for a little extra credit:

- Implement a capacitive DAC with output buffer to replace the PWM DACs the digital guys are making.

- Add power-gating to as much of your design as possible. What is the leakage when everything is off? How long does it take after turn-on for, e.g., the PGA to be stable enough to use?

- Add a power-on reset circuit, brown-out detector circuit, or other supply monitoring.

- Simulate the noise in one or more of your blocks

- Generate the clocks for one or more of your analog blocks

Collaboration vs. Cheating

You are encouraged to discuss your ideas with other project groups, and help each other with your designs, but there are limits. **Do** help each other debug SPICE problems, but **Don't** share SPICE decks or cadence schematics. **Do** brainstorm on topologies, calculations, and design ideas, but **Don't** jointly agree on what all the saturation voltages, drain currents, and W/L values should be. Designers from Red Farm ICs are always lurking around trying to steal our designs!

Turn-ins

All of your cadence files are due by online submission on the due date on page 1. That represents your FINAL DESIGN. Your final presentation is due by electronic submission before you get on stage to present it.

Early turn-in bonus: 10% extra credit if the FINAL DESIGN is turned in by Friday 4/28/2017 at 9AM. Extra credit is pro-rated linearly from 10% to 0% between that time and the due date.

References

[1] Scott, Boser, Pister, "An Ultra-low Energy ADC for Smart Dust", JSSC, V38N7, 2003.

http://en.wikipedia.org/wiki/Successive_approximation_ADC

http://en.wikipedia.org/wiki/Switched_capacitor

Common Acronyms

ADC   Analog to Digital Converter

DAC   Digital to Analog Converter

LSB   Least Significant Bit

PGA   Programmable Gain Amplifier

PTAT   Proportional to Absolute Temperature

PWM   Pulse Width Modulation

SAR   Successive Approximation Register, the digital block that controls the ADC