EE140: Lab 1 Exploring a lousy op-amp

Due: Week 3, Feb. 1-5, 2017

Introduction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You may obtain data in pairs, but must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision. Don't use a calculator – I won't let you use one on the exam and it's good to get in practice.

Objective

This lab is meant to get you thinking about regions of operation of transistors, and how the bias point, or operating point, affects circuit performance. Other goals include learning about input offset voltage, common mode input range, and that even lousy op-amps can be useful in some applications. You'll also learn to use LTspice (or any other spice that you want to use) if you don't know already.



Figure 1: Lab 1 Op-Amp [File: 2T2Ropamp.asc]

Prelab (stuff done before the lab. No seriously. If possible.)

HAND ANALYSIS

For the circuit in Figure 1, assume that V+=V=0. You can assume that $V_{BE,ON}=0.7V$, and that V_A is infinite. All of the following should be in the writeup:

- 1. Calculate V_{tail} , I_{tail} , I_{C2} . and Vout. It should be easy if you do it in that order. V_{out} should be about $V_{BE,ON}$. (say what? how can that be? explain!)
- 2. Calculate g_{m2} . You should get about 0.1S
- 3. Calculate the gain from V+ to Vout, which is roughly $g_{m2}R_{load}/2$

SPICE

- 1. Install LTspice IV on your computer. It's free, and runs on Windows and Mac. <u>http://www.linear.com/designtools/software/</u> Any other spice simulator is fine as long as it can simulate BJTs and op-amps (ideally the ones that you'll be using, 2N3904, 2N3906, and LM324).
- 2. Run the DC sweep on the amplifier in figure 1.
 - a. Run LTspice. Open 2T2Ropamp.asc . Click the little running guy icon. This runs a DC sweep from Vin = -6V to +6V. The horizontal axis is Vin.
 - b. Click on the input wire (V+). You should see a diagonal line in the plot. That's plotting Vin against itself.
 - c. Click on the Vtail wire. You should see a second trace which is stuck at roughly -0.7V on the left, and then follows Vin about 0.7V below it on the right.
 - i. [Writeup] Explain why the two regions look like they do.
 - ii. [Writeup] Roughly what range of Vin will put Q1 in forward active, and what range of Vin will put Q2 in forward active?
 - iii. [Writeup] Is there a region where both devices are in forward active? What would you guess about the quality of performance of the op-amp inside and outside of this region.
 - d. Click on the out wire. Zoom in on the region near Vin=0. In the plot window, click on the label on the top that says "V(out)". This will give you a cursor that you can drag around. Click it again and you get a second one, and LTspice will calculate gain for you. The gain changes a lot between Vin=0V and Vin=0.1V. Put the two cursors about 10mV apart near Vin=0.
 - i. [Writeup] What is the voltage gain near Vin=0? How does that compare to your hand calculation?
 - ii. [Writeup] What is the voltage gain near Vin=0.1V? Why do you think it is so much lower? [hint: think gold mines in hw1]
- 3. Load and run the circuit in 2T2RopampFB.asc .
 - a. [Writeup] Draw the op-amp as a triangle with R1 and R2 in feedback around it. What gain do you expect from this amplifier?
 - b. After you run the simulation, click on the input, V+, and the output, out. Measure the gain with the cursors close together.
 - c. [Writeup] What is the range of Vin over which the gain is within 10% of the ideal op-amp value that you calculated in part a?
 - d. Click on V-. [Writeup] Why is it following V+ (what causes it to do that)?
 - e. Click on Vtail. [Writeup] Estimate the range of Vin for which both transistors are in forward active.

Lab

- 1. Build the circuit in *Figure 1*.
- 2. Measurements
 - a. DC Biases
 - i. Ground the inputs and measure the tail and output voltages. Make sure that they are consistent with your hand calculations, and simulations.
 - ii. Debugging tip: always start by checking that your supplies are where you think they are. Measure from ground to each supply, and from the bottom to the top.
 - b. Keep the negative input grounded, and sweep the positive input from -6 to +6V (or as close to that as you can. The waveform generator should be able to do it with a triangle wave).
 - i. Take a picture of the results. Compare to the spice plot and comment on any differences.
 - ii. Zoom in near Vin=0 and estimate the peak gain. Compare to your hand calculation.
 - iii. Show both of these to your TA. TA initials
 - c. Resistive Feedback
 - i. Connect resistors R1 and R2 in feedback from Vout to V.
 - ii. Perform the same DC sweep as above, and try to identify the range of Vin for which the gain is within 10% of 2.
 - iii. Show your results to your TA. TA initials______
 - d. Unity gain feedback.
 - i. Remove R2
 - ii. Perform the same DC sweep as above, and try to identify the range of Vin for which the gain is within 10% of 1.
 - iii. Show your results to your TA. TA initials_____
 - 3. Now we'll add a second stage.
 - a. Run 3T3Ropamp.asc, build that circuit, and do part 2b again. (Note that positive and negative inputs have switched with the addition of a second stage with negative gain.)
 - b. Run 3T3RopampFB.asc, build that circuit, and try to do part 2c. You may see oscillations. Reduce the feedback factor (increase the closed-loop gain) until the oscillations go away.
 - c. Try unity gain feedback with the 3T3R opamp. You should definitely see oscillation. What frequency and amplitude do you see? We'll spend a lot of time figuring out how to keep two-stage op-amps from oscillating.

In your writeup, try to explain what is going on with the various node voltages as the input sweeps from -6 to +6. What performance do you expect from an ideal op-amp? How does that differ from what you built? Why do the node voltages change the way that they do, especially when they aren't doing what you want from an ideal op-amp perspective?



E Figure 2: BJT Pin Configuration