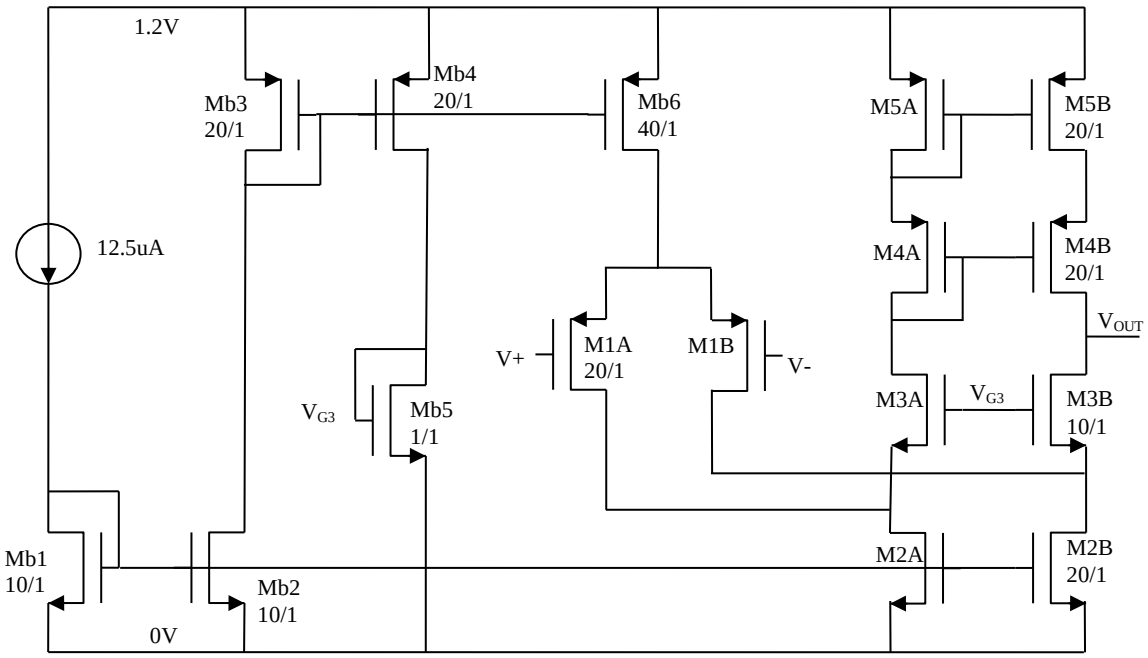
EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #9

Due by online submission **Tuesday** 4/11/2017 (Wednesday 9am)

1. For the PMOS-input folded cascode op-amp below, assume quadratic model and the following process specs $\mu_n C_{ox}=250\mu A/V^2$, $\mu_p C_{ox}=125\mu A/V^2$, $\lambda=1/(10V)$, $-V_{tp}=V_{tn}=0.2V$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$.



   a. Calculate and tabulate:
      i. the overdrive voltage and current in all devices. For this step you may assume that $\lambda=0$. The simplest order may be Mb1 through Mb6, then M1 through M5.
      ii. Calculate the bias voltages on all nodes, assuming $V_{I,CM}=1V$. Specifically: tail, G2, G3, G5, G6, S3B, S4AB, and out.
      iii. the g_m and r_o parameters for M1 through M5
   b. Calculate Gm, Ro, and Av
   c. Calculate the input common mode range and output swing.
   d. What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing?
   e. If the load capacitance is 1pF (roughly ten times the input capacitance),
      i. what is the dominant pole frequencies?
      ii. What are the frequencies of the pole/zero doublets from the current mirror?
      iii. What is the pole frequency of the common gate (cascodes) 3AB?
      iv. What is the unity gain frequency?
      v. What is the phase margin?
2. To increase the positive output swing of the previous amplifier,
   a. redraw the PMOS current mirror M4AB, M5AB as a high-swing cascode current mirror, as in Figure 5.18b in Razavi (5.13b in the 1st edition), but PMOS.
   b. Generate V_b (V_{G4}) using something like Mb5 above, but PMOS. What current source do you use? What gate voltage biases it? What W/L do you use for all devices, and why?
   c. [240A] generate V_b from the circuit suggested in 5.19b in Razavi. What value for $(W/L)_5$ in that figure is needed?
3. In Figure 2 of this Analog Devices discussion on voltage regulators
   http://www.analog.com/en/design-center/landing-pages/001/fundamentals-of-ldo-design-and-applications.html
   a. Why does the SENSE value connect to the positive input of the op-amp? Is this positive feedback?

   b. Estimate the feedback factor f, and the regulated voltage V_{out}, assuming a load resistance R_L (not shown in the figure), and the SENSE and VOUT pins shorted.
   c. Estimate the low-frequency loop gain T in terms of the op-amp voltage gain A_0, g_m of the pass transistor, and load resistance R_L.
4. For the circuit in figure 13.6 in Razavi
   a. what ratios of C_1 to C_2 are needed to make a variable gain amplifier with gain equal to any integer between 1 and 8?
   b. for a given open-loop op-amp gain A, which of the closed-loop gains above has the worst gain error?
   c. if the desired closed-loop gain accuracy is 0.4% regardless of gain setting, what is the minimum open-loop gain necessary for the op-amp?
   d. if the amplifier must settle to within 0.4% of the correct value within 10us, what is the minimum unity gain bandwidth of the op-amp?
5. In the TI document on SAR ADCs, http://www.ti.com.cn/cn/lit/an/slyt176/slyt176.pdf
   a. does the comparator compare at ground or the top rail?
   b. Assuming a single-sided supply (V_{DDA}, 0) does the voltage on the inputs to the comparator stay between the supply rails?
6. [ee240A] For the amplifier in problem 1, how does performance change
   a. if the bias current drops to 1uA and all devices are biased at roughly $V_{gs}=V_t$?
   b. if the bias current remains 10uA, but the length of all devices is changed to 14nm, and the widths vary from 20nm to 40nm as appropriate for a current density of 0.5mA/um? Use your answers to problem 4 of Homework 2 (the Intel FinFET paper). Assume that the load capacitance is ten times the input capacitance (which is?).