EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #7

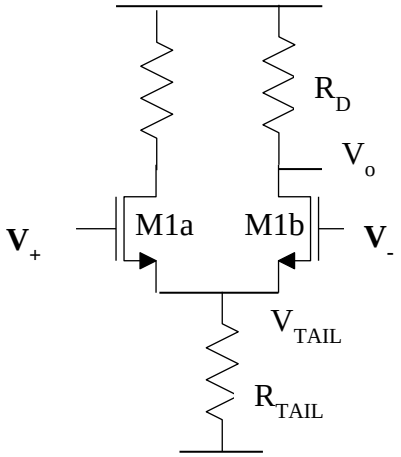
Due by online submission Wednesday 3/15/2017 (Thursday at 9am)

1. Check out the datasheet for the K2-W tube op-amp. This op-amp, released in 1952, was the first production op-amp. It runs from a +/-300V supply, and has a BW of 300kHz (or k-cycles/s, as they said back then – the unit Hertz not having been established yet). There's a schematic on page 2. Pins 1, 2, and 6 on the bottom of the figure are V+, V-, and Vout. VR1 and VR2 are neon bulbs that provide a low impedance level shift of roughly 100V to center the output between the rails. Identify (circle and label):
    a. input differential pair
    b. diff-pair load resistor
    c. tail current resistor. Estimate the common mode gain of the first stage and write it near the tail resistor.
    d. Common-cathode gain stage (like CS or CE)
    e. Cathode-follower output stage (like source-follower or emitter follower, CD, CC)
    f. Miller-multiplied compensation capacitor from the output back to the input of the gain stage.
    g. Bonus points if you can identify positive feedback in this amplifier, designed to increase the low-frequency gain (which ended up at about 20,000).
2. Estimate the output resistance of a CMOS differential amplifier with current mirror load. You may assume that $g_m r_o >> 1$ for all combinations of g_m and r_o. The following steps may help.
    a. Estimate the impedance seen looking into the source of M1A
    b. Estimate the impedance seen looking down from the source of M1B
    c. Estimate the impedance seen looking into the drain of M1B
    d. For the Ro calculation, estimate i_{d1B} as a function of vo.
    e. The current in i_{d2B} is due to both the output resistance and the mirrored current. Estimate both parts.
    f. Estimate the total output current io = $i_{d1B} + i_{d2B}$
    g. Show that R_o. is equal to ($r_{o1B} \parallel r_{o2B}$). Magic!
3. Design a 2-stage NMOS input CMOS op-amp with the following specs:
    a. 200uA tail current
    b. able to sink 1mA from the load
    c. output swing to within 200mV of the rails
    d. input common mode range to within 200mV of the top rail, and 1.4V of the bottom rail.

Process specs $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda=1/(10V)$, $-V_{tp}=V_{tn}=1V$, $V_{DD}=5V$, $L_{min}=0.5um$, $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$. You may use 1 resistor in your design.
Draw the schematic, label the device size of each transistor and the bias current flowing in each leg.

4. For the amplifier in the previous problem,
    a. Calculate the variation in tail current over the common mode input range.
    b. Assuming Vic=2.5V, calculate and tabulate I_d, V_{ov}, g_m, r_o, for all devices; and C_{gs}, and C_{gd} for all devices in the signal path
    c. calculate the 1st and 2nd stage gain, and the overall gain for both differential and common mode signals.
    d. Calculate the uncompensated 1st and 2nd stage pole locations with a 1pF load
    e. Calculate the compensation capacitor necessary for 45 degree phase margin with a 1pF load (ignoring the effect of the RHP zero) and the resulting compensated pole locations
    f. Sketch a Bode plot of the gain with a 1pF load capacitance, including the RHP zero, and the mirror pole/zero doublet.
5. For the differential amplifier in the figure below, estimate the change in V_{tail}, I_{tail}, I_{d1a}, I_{d1b}, and Vo due to

a. An increase of ΔV in both V+ and V-
b. An increase of ΔV in just V+
c. An increase of ΔV in just V-
d. What is the common mode rejection ratio of this amplifier?



6. [240A] Show that the gain from v_{id} to v_{tail} in a diff pair with a current mirror load is +1/4.