Homework Assignment #6
Due by online submission **Thursday** 3/9/2017 (9am Friday)

1. Check out the "early op-amp" in Figure 2 on this page https://www.maximintegrated.com/en/app-notes/index.mvp/id/4428 .
   a. [5] Circle and label the following components
      i. differential pair with resistive load
      ii. tail current sink
      iii. common emitter gain stage with level-shifting diodes
      iv. output stage with current-limiting resistors
      v. Zener diode based voltage reference
   b. [1] Why is there a resistor in series with the Zener diode?
   c. [2] If the Zener has a reverse breakdown of 3.5V, and the tail resistor is 1kΩ, what is the tail current? Does it vary much with supply voltage?
   d. [1] If you were going to add a compensation capacitor to this op-amp, where would you put it? (draw it on the circuit)
2. Check out the datasheet for the LM324 quad op-amp. http://www.ti.com/lit/ds/symlink/lm324.pdf TI has been selling this op-amp for more than 40 years! (they are $0.09 each on digikey) There's a schematic on page 10. Copy that schematic, and identify (circle and label)
   a. input differential pair (Darlington)
   b. current mirror active load
   c. compensation capacitor
   d. common collector level shifter (emitter follower)
   e. common emitter amplifier (Darlington)
   f. output stage
3. From Figure 4 on the LM324 datasheet
   a. estimate the slew rate in positive and negative slewing when the output load is 50pF
   b. we haven't studied output stages, but you can find the output current limits in the table on page 7. Is the slew rate due to the output capacitor?
   c. estimate the size of the compensation capacitor C_c
4. Same circuit, different manufacturer: https://www.onsemi.com/pub/Collateral/LM324-D.PDF
   a. What are A_{vo} (not in dB), ω_{p1}, and ω_u? (Hertz or rad/sec, but use f or ω appropriately) (Figure 6)
   b. Estimate the location of the second pole when the load capacitance is 1,000pF (Figure 4)
5. The LT1008 http://cds.linear.com/docs/en/datasheet/1008fb.pdf (also decades old, $3.55 on digikey) is not internally compensated. This gives you higher performance (BW, slew rate) for higher gain, but means that you need to add external capacitance when using the amplifier in low-gain configurations. They give you two choices, either add a capacitor C_F that will be somewhat Millerized or add C_S that looks more like our C_2.
   a. with a closed loop gain of 1,000 and perfect feedback resistor matching,
      i. estimate your gain error at 0.1 Hz
      ii. estimate the closed-loop pole location with C_S=10pF vs. C_F=30pF (page 6, lower left)
   b. With CF=3pF vs. 30pF, what is the maximum feedback factor (and corresponding minimum gain and max bandwidth) that will give a phase margin of 60? (page 6, lower right)
6. Figure 6.15 in the book is a model of a two-stage amplifier.
   a. re-draw it using our terminology from class: G_{m1}, G_{m2}, R_{o1}, R_{o2}, C_1, C_2, C_c.
   b. Equation 6.30 is the transfer function of the amplifier. Re-write that with our terminology.
   c. Equation 6.39 is the simplified expression for the 2nd pole location, assuming the first pole is given by Miller-multiplied Cc.
      i. Re-write that with our terminology

ii. Assuming that the 2nd stage gain is much larger than 1, the Miller capacitance is all that matters in the compensated first stage pole $\omega_{p1,c}$, write the expression for the compensated second stage pole $\omega_{p2,c}$ in terms of only capacitors and the transconductance of the second stage.

iii. With those same assumptions, and ignoring any other poles and zeros, what is the constraint on transconductance and capacitance that insures a unity gain phase margin of at least 45?

7. [240A] In the "early op-amp" above,
   a. if the current-limiting resistors are small, estimate the gain of the output stage as a function of output current to/from the load
   b. if the two diodes are implemented as diode-connected versions of the two output transistors, the current limiting resistors are 10 Ohms, and the output is grounded (or connected to a very low impedance load to ground), sketch the output current as a function of the collector voltage on the common emitter gain stage, over a +/-2V range.