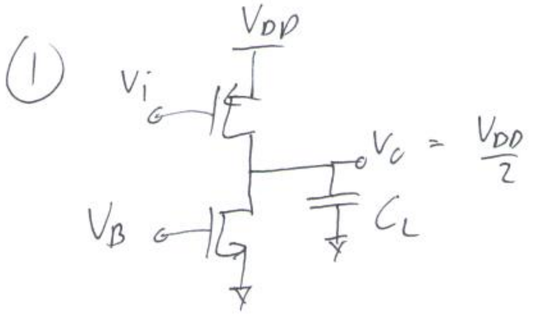
EE 140 HW 4

①



24 pts
+1 per entry

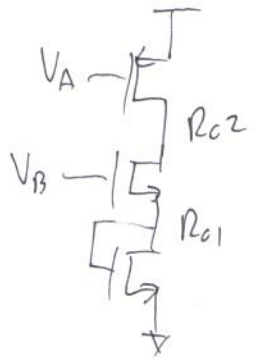
Change	I_D	gm	r_o	A_v	ω_p	ω_n	C_{in}	swing
2×W	2x	2x	$\frac{1}{2}$x	1x	2x	2x	2x	1x
2×W, 2×L	1x	1x	2x	2x	$\frac{1}{2}$x	1x	4x (1)	1x
2×V_{ov}	4x	2x	$\frac{1}{4}$x	$\frac{1}{2}$x	4x	2x	$\frac{1}{2}$x - 1x (2)	$\frac{1}{2}$x

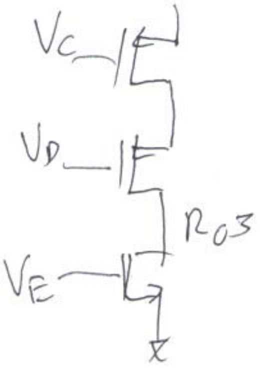
(1) If C_{gs} dominates, $C_{gs} = \frac{2}{3}(2W)(2L)C_{ox} \rightarrow$ 4x increase

If C_{gd} dominates, $C_{gd} = C_{ol}' W \cdot 2 \rightarrow$ 2x increase, but gain also went up 2x so still 4x increase.

(2) C_{gs} doesn't change but Miller-multiplied C_{gd} drops to $\frac{1}{2}$x.

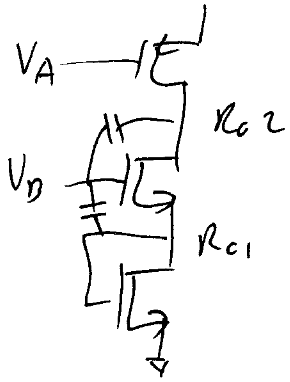
② Problem 5 from F09 midterm 1





②

b) low freq cap into V_B ?



$$A_{VB\to1} = G_m R_o$$

$$G_m = \frac{g_m}{1+g_m\frac{1}{g_m}} = \frac{g_m}{2}$$

from a) know $R_{o1} \approx \frac{2}{3}\frac{1}{g_m}$

$$A_{VB\to1} = \frac{g_m}{2}\,\frac{2}{3}\,\frac{1}{g_m} = \frac{1}{3}$$

(b) 4 pts total
+2 for finding both Miller gains
+2 for getting correct Cin expression

$A_{VB\to2}$:

$$G_m = \frac{g_m}{1+g_m\frac{1}{g_m}} = \frac{g_m}{2}$$

$R_{o2} = \frac{2}{3} r_o$ (from (a))

$$A_{VB\to2} = -\frac{g_m}{2}\,\frac{2}{3}\,r_o = \frac{-g_m r_o}{3}$$

$$C_{in} = \left(1-A_{VB\to1}\right)C_{gs} + \left(1-A_{VB\to2}\right)C_{gd}$$

$$\boxed{C_{in} = \frac{2}{3}C_{gs} + \left(1+\frac{g_m r_o}{3}\right)C_{gd}}$$

(a) 8 pts total
+1 each for ro_up, ro_down, and ro_total
+1 setting up equations for Cin
+1 for finding correct Cin

$$R_{o1,up} = \frac{r_o + r_o}{1+g_m r_o} \approx \frac{2}{g_m}$$

$$R_{o1,down} = \frac{1}{g_m}$$

$$R_{o1} = \frac{2}{g_m} // \frac{1}{g_m} = \frac{2}{3 g_m}$$

$$R_{o2,up} = r_o$$

$$R_{o2,down} = r_o + (1+g_m r_o)\frac{1}{g_m} \approx 2r_o$$

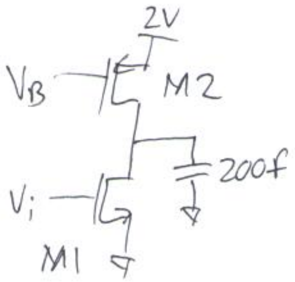
$$R_{o2} = r_o // 2r_o = \frac{2}{3} r_o$$

$$R_{o3,up} = g_m r_o^2$$

$$R_{o3} = r_o$$

$$R_{o3,down} = r_o$$

③ $|A_v| = 50 \text{ V/V}$ $\omega_u = 2\pi \, 1.6\,G$ $C_L = 200fF$ swing $= 1V$



$$\omega_u = \frac{g_m}{C_L}$$ $$g_m = (2\pi \, 1.6 \, 10^9)(2 \, 10^{-13}) \approx 2mS$$

$$A_v = \frac{1}{\lambda V_{ov}}$$ Choose $V_{ov} = 200mV$ (for both NMOS & PMOS)

then need

$\lambda \leq 0.1 V^{-1}$

$\lambda = \frac{0.1um}{L} \frac{1}{V}$ so $L = 1um$

$$g_m = \frac{2 I_D}{V_{ov}}$$ $$I_D = \frac{g_m V_{ov}}{2} = 200uA$$

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 \qquad W = \frac{2 I_D L}{\mu C_{ox} V_{ov}^2}$$

$W_n = 100\,\mu m$

$W_p = 200\,\mu m$

17 pts
+1 per entry in M1/M2 design table
+1 per entry in Av,wp,wu,Cin,swing table

	W	L	I_D	V_{ov}	gm	r_o
M1	100um	1um	200uA	0.2V	2mS	50kΩ
M2	200um	1um	200uA	0.2V	2mS	50kΩ

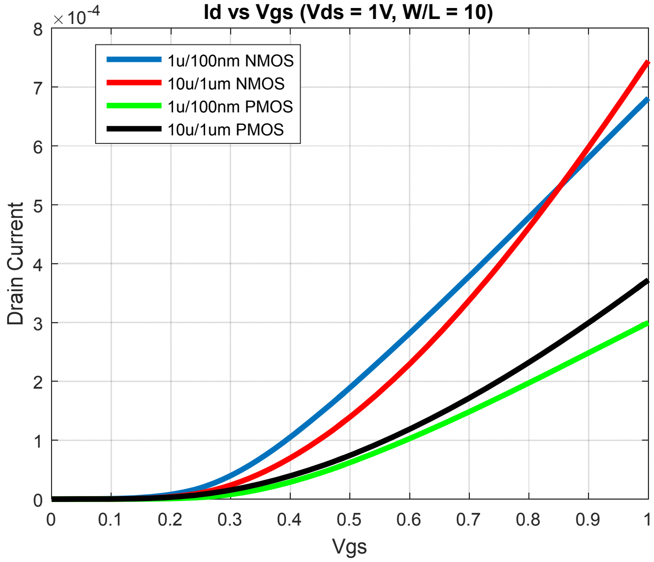
A_{vo}	ω_p	ω_u	C_{in}	swing
50 V/V	24MHz	1.2 GHz(1)	1.35pF	1.6 V

$$C_{in} = C_{gs} + (1+A_v) C_{gd} = \frac{2}{3} WL C_{ox} + 51 C_{ol} \cdot W$$

(1) Note that we don't meet the bandwidth spec because $C_{gd} \approx 60fF$ in total (NMOS + PMOS) at the output node which is signifant compared to 200fF.

The only way to get the bandwidth with a common source would be to make the devices so large that $C_{gd} \gg C_L$ which is impractical.

P4) a)



4a) 4 pts. Full credit for noting that the short channel devices look mostly velocity saturated, and that the long channel devices look quadratic over some range.

Short channel devices do look linear as expected in velocity saturated devices. The long channel devices look mostly quadratic. They look like they start to turn linear near the higher values of Vgs (~0.8V).

b) We can find Vt by choosing two (Vgs,Id) pairs on the curve and dividing them.

For the NMOS:

$$\frac{I_{D1}}{I_{D2}} = \frac{(Vgs1 - Vt)}{(Vgs2 - Vt)} = \frac{378uA}{580uA} = \frac{0.7V - Vt}{0.9V - Vt}$$

Which results in **Vtn = 325 mV.**

4b) 4 pts. Full credit for attempt at estimating Vt and CoxVscl from slope

For the PMOS:

$$\frac{I_{D1}}{I_{D2}} = \frac{(Vgs1 - Vt)}{(Vgs2 - Vt)} = \frac{149uA}{248uA} = \frac{0.7V - Vt}{0.9V - Vt}$$

Which results in **Vtp = 400 mV.**

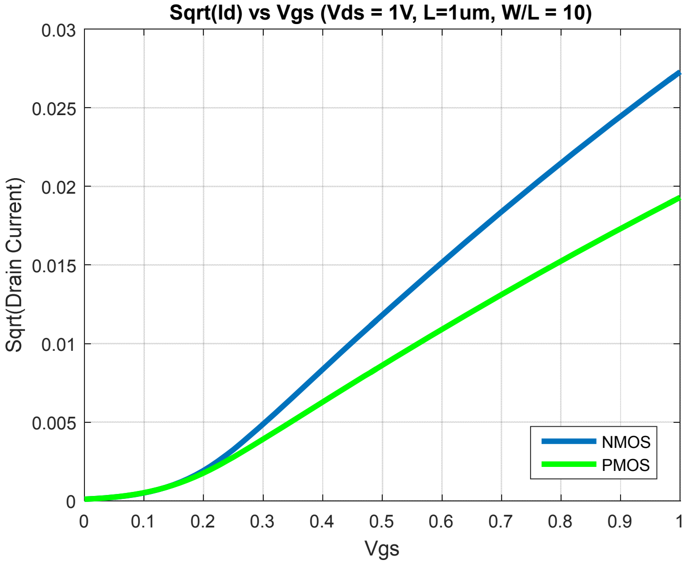
We can find Cox*Vscl for the NMOS by:

$$Cox * Vscl = \frac{I_D}{W(Vgs - Vt)} = \frac{429uA}{1um(0.75V - 0.325V)} = \mathbf{1000}\ \frac{\boldsymbol{A}}{\boldsymbol{um\ V}}$$

For the PMOS:

$$Cox * Vscl = \frac{I_D}{W(Vgs - Vt)} = \frac{173uA}{1um(0.75V - 0.400V)} = \mathbf{500}\ \frac{\boldsymbol{A}}{\boldsymbol{um\ V}}$$

c)



Using the same approach as (b) and choosing points on the straight portion of the curve:

For the NMOS:

$$\frac{\sqrt{I_{D1}}}{\sqrt{I_{D2}}} = \frac{(Vgs1 - Vt)}{(Vgs2 - Vt)} = \frac{0.0101}{0.03149} = \frac{0.45V - Vt}{0.55V - Vt}$$

Which results in **Vtn = 400 mV.**

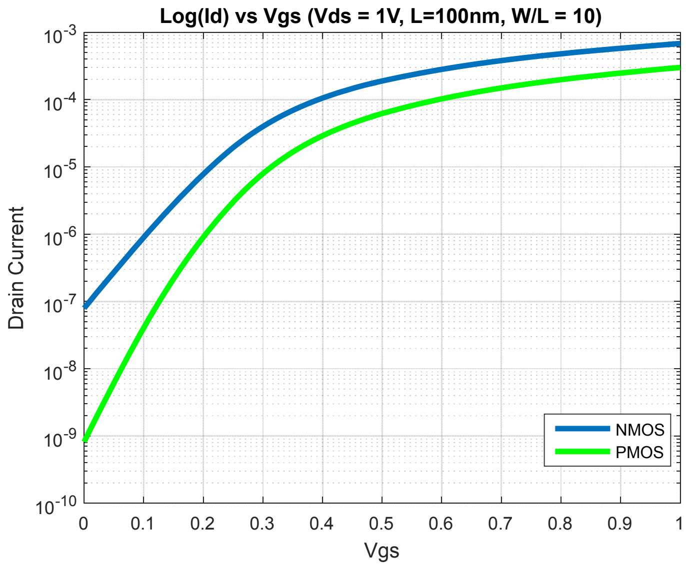
4c) 4 pts. Full credit for the right approach (slope of curve)

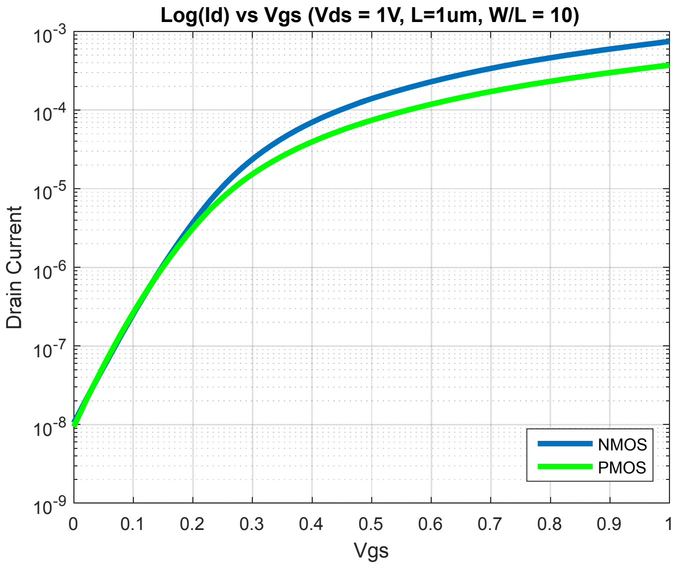
For the PMOS:

$$\frac{\sqrt{I_{D1}}}{\sqrt{I_{D2}}} = \frac{(Vgs1 - Vt)}{(Vgs2 - Vt)} = \frac{0.007461}{0.00977} = \frac{0.45V - Vt}{0.55V - Vt}$$

Which results in **Vtp = 114 mV.** (note that this seems too low)

d)





For the short channel devices (left plot),

The NMOS slope is:

$$\frac{0.105V - 10mV}{decade} = 95mV/dec$$

Which yields **n=95/60 = 1.58** for the short channel NMOS.

4d) 2 pts. Full credit for right approach (n*60mV/decade = 1/(slope of curves))

The PMOS slope is:

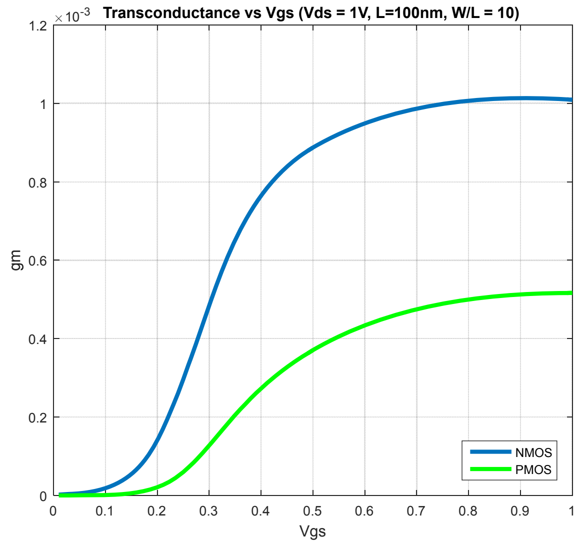
$$\frac{0.065V - 5mV}{decade} = 60mV/dec$$

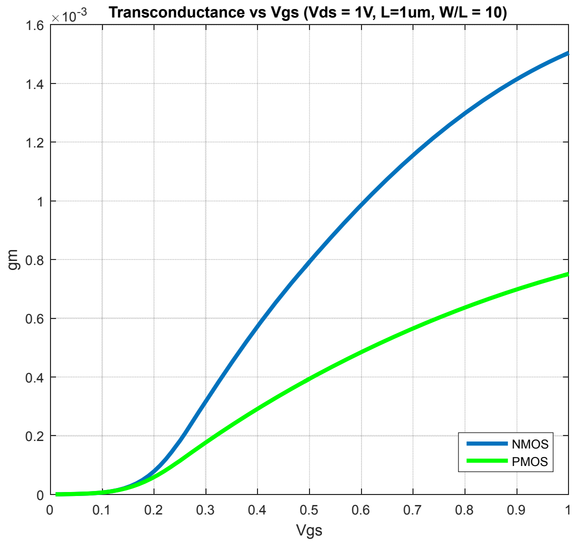
Which yields **n=60/60 = 1** for the short channel PMOS. Note that this model shows that the PMOS is as good as a BJT; it can't get any better than this.

For the long channel devices (right plot), they both have nearly the same slope of 70mV/decade.

Which yields **n=70/60 = 1.2** for the long channel NMOS and PMOS.

e)



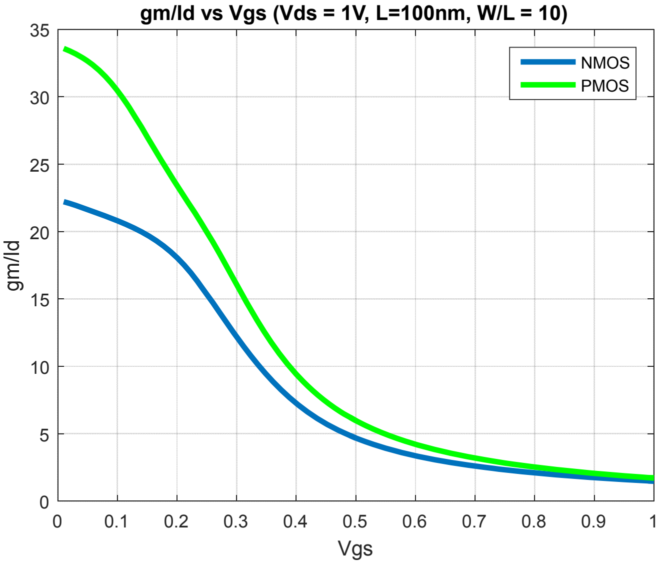


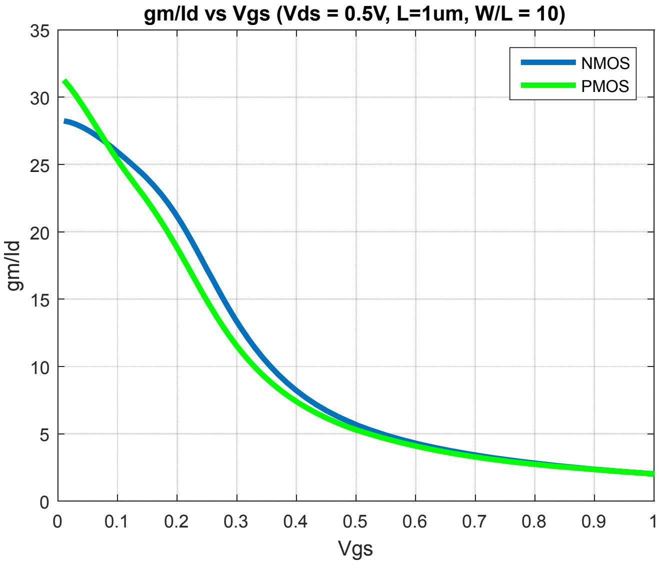
For short channel devices (left) we expect to see that gm becomes constant when velocity saturation is reached, which appears to begin happening somewhere around Vgs of 0.4V (which is a higher field than the expected 1V/um).

For long channel devices (right) gm should linearly increase with Vgs which appears to be mostly the case here until we begin reaching higher values of Vgs. Our 1V/um model says the long channel devices should saturate at Vgs=1V.

4e) 4 pts.
--> 1 pt each for saying that short channel (vel. sat model) should be constant, long channel (quadratic model) should be linear in Vov
--> 1 pt each for giving a reasonable range for short and long.
--> 2 pts for saying something related to field to explain why.

f)

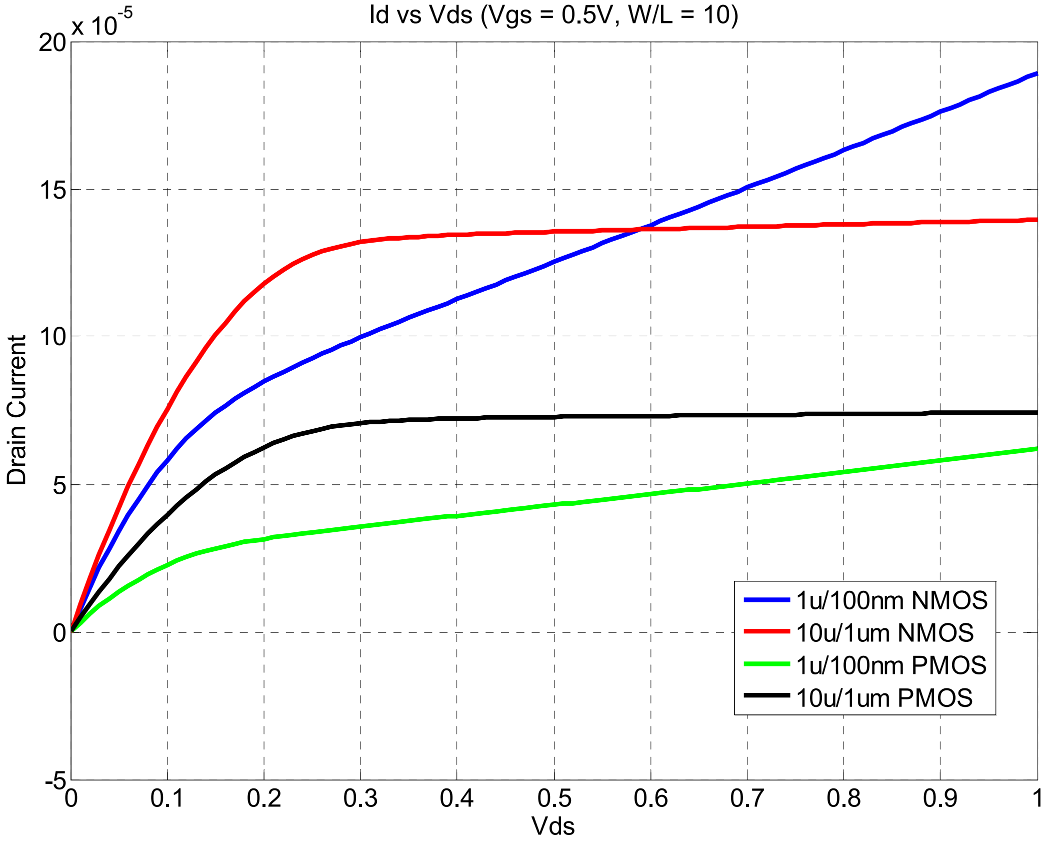




The short channel PMOS in subthreshold appears to be the best, closely followed by both of the long channel devices, also in subthreshold.

4f) 2 pts. Full credit for plots and choosing highest gm/Id

P5)



There appear to be visible transitions from saturation to triode for all devices. For the short channel devices vdsat appears to be about 0.2 V while the long channel devices have vdsat ~0.3V.

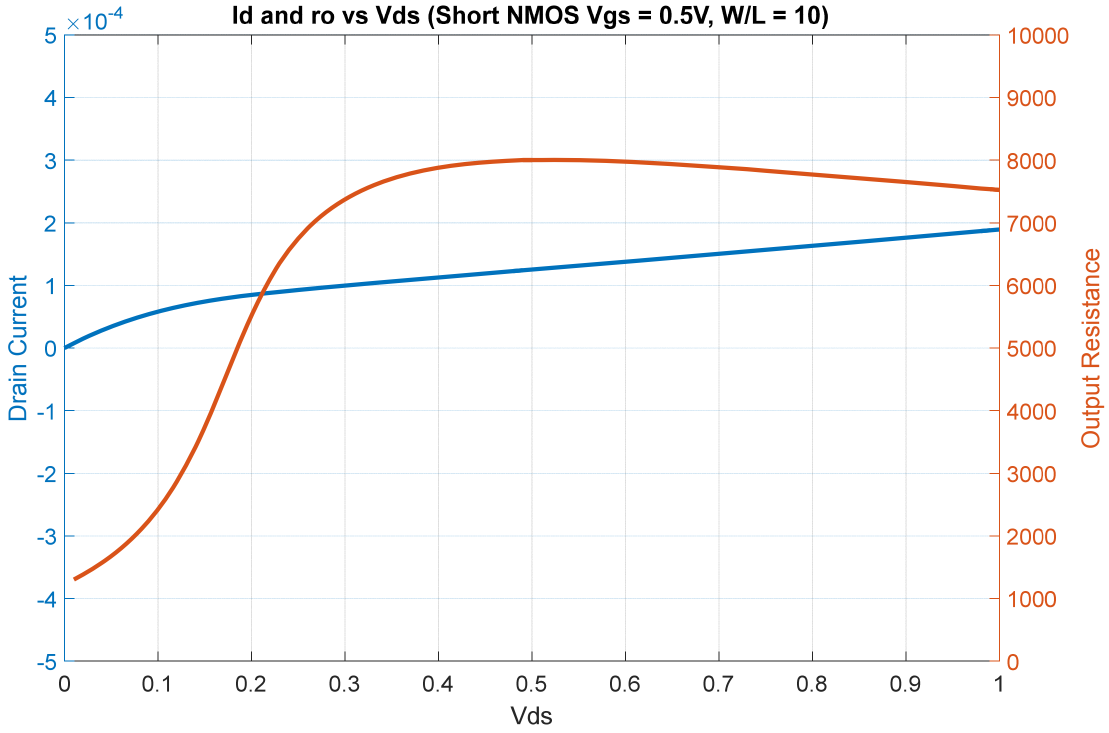
Extrapolating linear region to intersect with the x-axis yields:

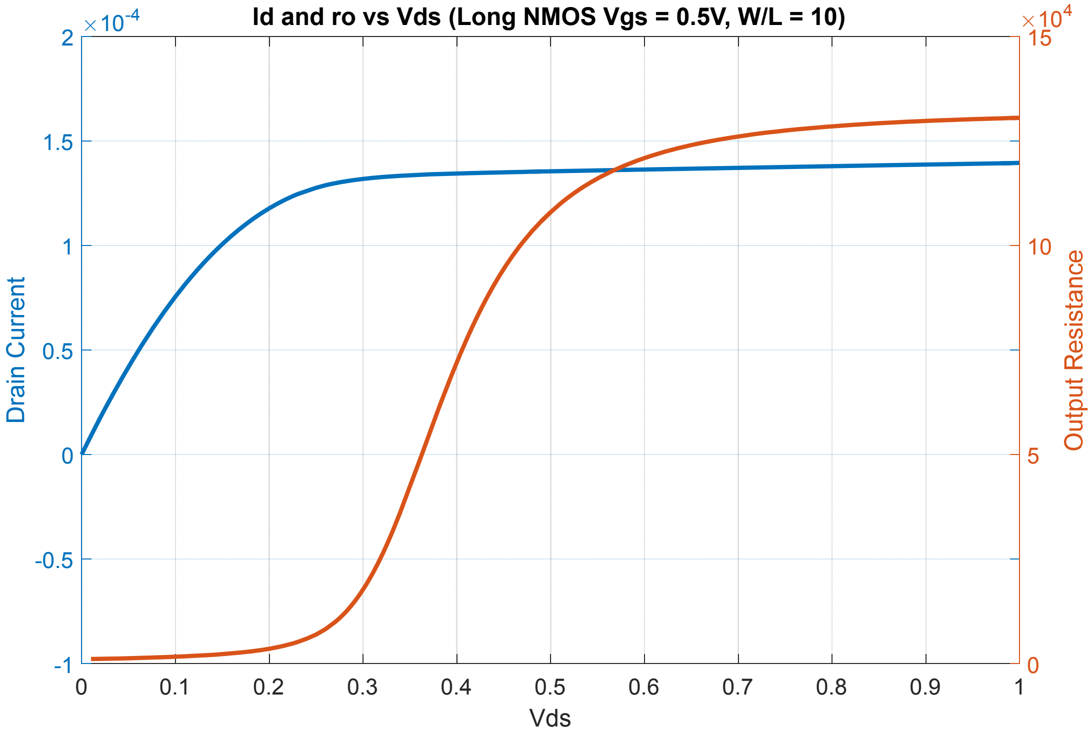
Device	VA
NMOS 1um/100nm	0.5 V
NMOS 10um/1um	16 V
PMOS 1um/100nm	0.7 V
PMOS 10um/1um	21 V

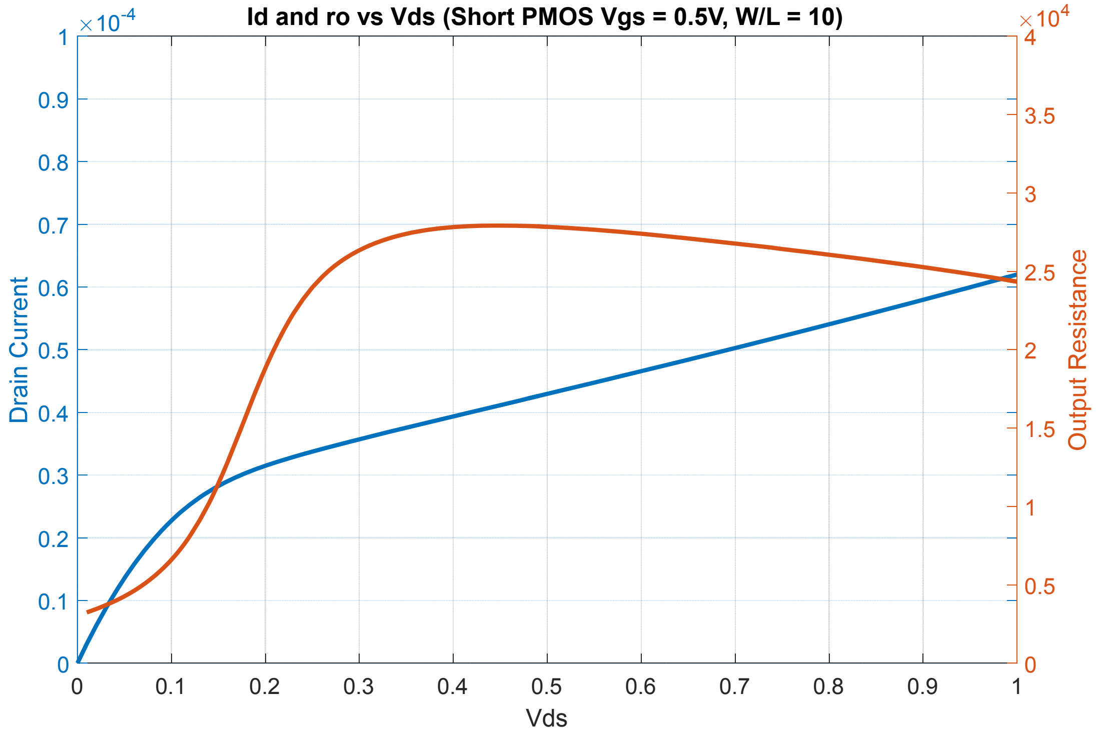
8 pts for part (a)
+2 for plot,
+2 for some discussion of triode/saturation for long vs short channel,
+1 (4pts total) for each of the four VA values within reasonable range

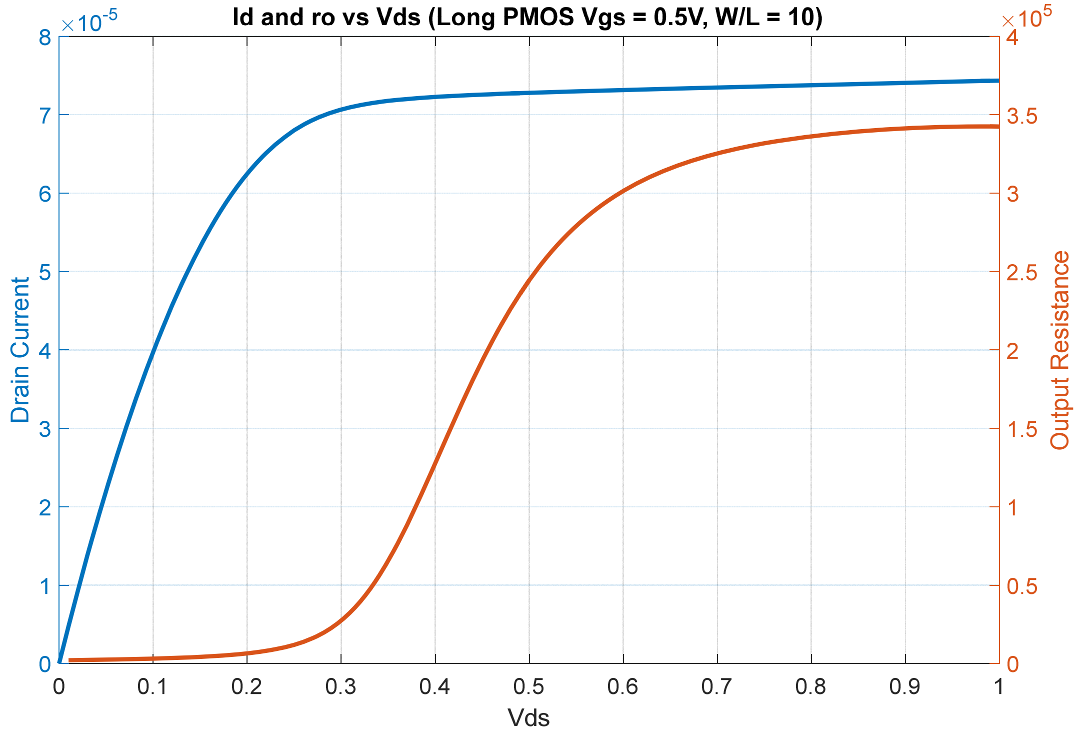
b)

4 pts +1 per plot


Id and ro vs Vds (Short NMOS Vgs = 0.5V, W/L = 10)


Id and ro vs Vds (Long NMOS Vgs = 0.5V, W/L = 10)


Id and ro vs Vds (Short PMOS Vgs = 0.5V, W/L = 10)
×10^-4
×10^4
Drain Current
Output Resistance
Vds
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0.5
1
1.5
2
2.5
3
3.5
4


Id and ro vs Vds (Long PMOS Vgs = 0.5V, W/L = 10)
×10^-5
×10^5
Drain Current
Output Resistance
Vds
0
1
2
3
4
5
6
7
8
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
0.5
1.5
2.5
3.5

c)

8 pts. +1/2 for each max ro and vds range
Reasonably close values are fine

Device	Max ro [Ohms]	Vds Range for >Ro/2
NMOS 1um/100nm	8k	>160mV
NMOS 10um/1um	130k	>390mV
PMOS 1um/100nm	28k	>170mV
PMOS 10um/1um	340k	>440mV

d)

Using $r_o = \frac{1+\lambda V_{DS}}{\lambda I_D}$ with lambda = 1/VA yields the following results.

Device	Ro @ Vds = 1 V
NMOS 1um/100nm	7.9k
NMOS 10um/1um	120k
PMOS 1um/100nm	27k
PMOS 10um/1um	300k

They match relatively well for the short channel devices and are within 10% or so for the long channel devices.

The long channel matching becomes much worse below Vds ~ 0.5V, while the short channel matches relatively well down to a lower Vds of 0.2 V - 0.3 V.

4 pts. Full credit for any answer showing some thought.

HW4 grading rubric

1) 24 pts total. 1 pt each for each value in each part.

2) 10 pts total
2a) 8pts
1 pt each for ro_up, ro_down, ro_total (6pts total)
1 pt for Cin equation
1 pt for correct Cin
2b) 2pt for setting up equations, 2 pt for correct Cin

3) 23 pts total.
17 pts for design process. 1 pt for each value in transistor table and 1 pt for each in spec table (Av,wp,wu,etc)
3a) 2 pts. Full credit for any discussion of channel field
3b) 2 pts. Full credit for some discussion of design choices that affect power
3c) 2 pts. Full credit for some discussion of design choices that affect capacitance

4) 20 pts total
4a) 4 pts. Full credit for noting that the short channel devices look mostly velocity saturated, and that the long channel devices look quadratic over some range.
4b) 4 pts. Full credit for attempt at estimating Vt and CoxVscl from slope
4c) 4 pts. Full credit for the right approach (slope of curve)
4d) 2 pts. Full credit for right approach (n*60mV/decade = 1/(slope of curves))
4e) 4 pts.
--> 1 pt each for saying that short channel (vel. sat model) should be constant, long channel (quadratic model) should be linear in Vov
--> 1 pt each for giving a reasonable range for short and long.
--> 2 pts for saying something related to field to explain why.
4f) 2 pts. Full credit for plots and choosing highest gm/Id

5) 20 pts total.
5a) 8 pts
+2 for plot,
+2 for some discussion of triode/saturation for long vs short channel,
+1 (4pts total) for each of the four VA values within reasonable range
5b) 4 pts. +1 per plot
5c) 4 pts. +1/2 for each max ro and vds range
5d) 4 pts. Full credit for any answer showing some thought.

240A only
P6) 10 pts
Half for coming up with a model.
Half for evaluating its accuracy.