EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #4

Due by online submission Wednesday 2/15/2017 (Thursday at 9am)

1. You have a PMOS-input common source amplifier with an NMOS load driving a capacitive load. The output is biased at mid-rail. How do I_D, g_m, r_o, A_{v0}, w_p, w_u, input capacitance, and output swing change if you
    a. double the width of both devices
    b. double the width and length of both devices
    c. double V_{ov} in both devices
2. Problem 5, Fa09 Midterm 1.
3. Using the process parameters below, design a common source amplifier with a low-frequency gain of at least 50, and a unity-gain bandwidth of 1.6 GHz while driving a 200fF load. You need an output swing of at least 1V. Make a table of W, L, ID, Vov, gm, ro, for each device, and of Av0, wp, wu, input capacitance, and output swing for the amplifier. You may assume the quadratic model for both FETs, but keep Vov greater than 100mV. Clearly indicate "picks".
    a. Is the quadratic model likely to be accurate for the bias conditions of your amplifier?
    b. If you wanted to minimize power consumption, how would your design change?
    c. If you wanted to minimize input capacitance, how would your design change?

Process Parameters: C_{ox}=5fF/um^2, C'$_{ol}$=0.2fF/um, $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ= (0.1um/L)/(1V), $-V_{tp}=V_{tn}$=0.5V, V_{DD}=2V

4. With $|V_{ds}|$=1V, use Cadence in our 90nm process to simulate I_d vs V_{gs} from 0 to V_{DD}=1 V for both N and P transistors with W/L= 1u/100n and W/L=10u/1u. (Both are 10/1 aspect ratio, one is short channel, one is long channel).
    a. Plot all of the currents. Do the short channel devices look like our velocity saturation model? Do the long channel devices look quadratic? Perhaps over some range of Vgs?
    b. For the short channel devices, estimate $C_{ox}v_{scl}$ and V_{th}
    c. Plot sqrt(Id) for the long channel devices (click on the calculator icon to do waveform math). Estimate μC_{ox} and V_{th} for both N and P devices.
    d. Plot log10(I_d) for all devices. Estimate n.
    e. Plot g_m for all devices (there's a "deriv" function). What do you expect to see for short channel and long channel devices? In what range of V_{gs} does the g_m of these devices look like it comes from a quadratic or velocity saturated model? Is that consistent with any critical E-field?
    f. Plot g_m/I_d for all devices. In what device, and at what operating condition, do you get the most bang for the buck (most g_m per mA)?
5. For the same devices as above, simulate I_{DS} vs V_{DS} from 0 to V_{DD}=1V with V_{GS}=0.5V.
    a. Plot all four currents on the same plot. Is there a clear transition from triode to saturation? Is it the same for short and long channel? Estimate V_A for each device.
    b. For each device, plot I_{ds} and r_o on the same plot.
    c. For each device, find the max r_o, and the range of V_{ds} for which $r_o > r_{o,max/2}$
    d. Is $(1+\lambda V_{ds})/(\lambda I_d)$ a good model for output resistance for any/some/all of these devices? Over what range of voltages?
6. [ee240A] Come up with a model for hand analysis for transistors of length 0.1 to 1um that gives your best guess at g_m and r_o as a function of geometry and bias. How accurate is it in terms of percent error?