EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #3.1

Due by online submission **Monday** 2/6/2016 (Tuesday 9am)

1. An NMOS common source amplifier has a 10V supply and a 10kΩ load in parallel with 100pF. Assume $\mu_n C_{ox}$=20uA/V2, W/L=10,000/1, V_{th}=1V, λ=0.01V. You should be able to do all of the calculations by hand (without calculators). One-ish significant digits is fine.
   a. Write an expression for I_D as a function of output bias point. How much does I_D change as the output voltage varies from 9V to 1V?
   b. What is the change in the input and overdrive voltage as the output varies from 9V to 1V?
   c. Write an expression for g_m and r_o as a function of output bias point.
   d. Write an expression for A_{v0} as a function of output bias point.
   e. For each of the output bias points {9V, 6V, 1V}, calculate the current in the device, g_m, r_o, A_{v0}, ω_p, and ω_u . Fill in a table with those columns.
   f. Plot the output response to a 1mV input step on 3 time scales: 1ns, 1μs, 1ms.
2. A common source amplifier has a resistive load R_L and λ=1/(10V). For parts b and c assume V_{DD}=2V, and the output bias point is 1V.
   a. At this bias point, if the resistive load has the same impedance as the output resistance of the transistor, what is the supply voltage V_{DD}?
   b. Now with V_{DD}=2V and a different load resistor, should we approximate the output resistance R_O as R_L or r_o ? Why? What error in output resistance do we get if we make that approximation?
   c. With that approximation, write an expression for the gain that involves only voltages and a constant (no resistances, transconductances, etc.)
3. A single-pole amplifier has a low frequency gain of 100. At 10MHz the gain is 20. What are the pole frequency and the unity gain frequency?
4. Fill in the following table. Each row represents a different single-pole amplifier.

A_{v0}	ω_p	ω_u		g_m	r_o	C_L
100	1M					1p
	10M	2G			100k	
		1G			1M	100f
	10	10M				10p

5. For the common source amplifier, assume $\mu C_{ox}(W/L)$=1mA/V^2 , $|V_t|$=1V, and λ=0.1V^{-1} for both devices.

A) Assuming V_{BP} = 1.8 V, calculate V_{dsatp} and I_{dp} at Vdp=V_{DD}-|Vdsatp| for the PMOS transistor.

B) Plot |Idp| vs. Vout. What is the minimum and maximum value for Idp with the PMOS device in saturation in this circuit?

C) What is the approximate value of V_i for which the PMOS device is just on the edge between the saturation and linear regions? (you calculated the current and output voltage at which this happens in part A above). Considering just the current/ voltage relationship for the NMOS device, plot Idn at this Vi on the same plot as step B.

D) What is the value of V_i for which the NMOS device leaves saturation? Again, considering only the NMOS device, plot Idn at this value of V_i on the same plot as B.

E) Based on these values, plot V_{out} vs V_i, paying careful attention to the location of the endpoints of the high gain region (calculated in parts C and D above).

F) Based on the (Vi, Vout) pairs that you calculated in C & D, what is the gain of the amplifier? What are the input and output range over which this gain is achieved.

G) Calculate the gain for this amplifier using the small signal model evaluated at 3 different operating points for Vout: the edges of the high gain region, and the center of the high gain region.