EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #2.1

Due by online submission Monday 1/30/2017 (Tuesday at 9am)

1. How much does V_T vary over the industrial temperature range, -40 to +85 C?
2. Do this problem without using a calculator. You have a bag full of identical diodes. You measure one and find that it will pass 10uA when a voltage of 600 mV is applied at room temperature.
   a. if you apply 626 mV at room temperature, what do you expect the current to be?
   b. if you apply 660 mV at room temperature, what do you expect the current to be?
   c. if you use a current source to push 1nA through the diode at room temperature, what voltage do you expect to see?
   d. if you use a current source to push 10uA through the device at -40C, what voltage do you expect to see?
   e. If you put 10 diodes in series and run 10uA through them, what voltage do you expect to see across all 10 diodes?
   f. If you put 10 diodes in parallel and run 10uA through the parallel combination, what voltage do you expect to see?
3. From the datasheet for the 2N3904,
   a. From figure 4 at 25C estimate the base-emitter voltage change required to increase the collector current by a factor of 10, from 0.1 to 1 mA, or 1 to 10 mA.
   b. Estimate the same thing, but at -40C and 125C
   c. Are your answers consistent with your answer to problem 1?
   d. At a constant current of 1mA, what is the change in the base-emitter voltage from -40 to 25 C, and from 25 to 125 C? What is the temperature coefficient of $V_{BE,on}$ in mV/K? Is it close to what we said a diode should be? Should it be?
4. Look at the 2014 paper on the Intel 14 nm FINFET.
   a. From Figure 5, estimate gm, ro, and intrinsic gain for NMOS and PMOS transistors when V_{GS}=0.5V and V_{DS}=0.5V (PMOS values are negative). Note: the vertical axis in Figure 5 is mislabeled! It should be mA/um, not A/um. Figure 6 is correct.
   b. From Figure 5, estimate roughly what V_{TH} is for NMOS and PMOS devices. Do these devices look quadratic, or velocity saturated? Why?
   c. From Figure 6, estimate the subthreshold slope and the parameter "n" for NMOS and PMOS devices.
5. For an NMOS transistor with W/L=100u/1u, with $\mu_n C_{ox}=100\mu A/V^2$, V_{DD}=3V, $\lambda=1/(10V)$, and V_{TH}=1V.
   a. Carefully sketch by hand the drain current vs. V_{DS}=0 to 3V at constant V_{GS}=0, 1, 2, 3V.
   b. Do the same for a PMOS transistor of the same size with the same parameters except V_{DS}=0 to -3V and V_t=-1V. You should get exactly the same plot, just rotated 180 degrees and with different axis labels.
6. For an NMOS transistor, roughly sketch
   a. I_D and g_m vs. W/L for constant $V_{GS}>V_t$.
   b. I_D and g_m vs. V_{GS} for constant W/L.
   c. V_{ov} and g_m vs. I_D for constant W/L
   d. W/L and g_m vs I_D for contant $V_{GS}>V_t$
7. [ee240A] Find a novel transistor in a research paper from the last five years. (e.g. a nanotube, nanowire, 2D material like MoS_2, organic, …) and characterize it along the lines of problem 3. What are the important small signal parameters, and over what range of voltages are they valid?