EE 140/240A Prof. Pister
Spring 2017

Homework Assignment #10

Not due ever!

1. Take a look at the ADC schematic on slide 9 of the "Working with ADCs, Op-amps and the MSP430" http://www.ti.com/lit/ml/slap123/slap123.pdf

   When S_1 and S_c are closed, and all capacitor bottom plate switches are in the green position,
   a. What is the total capacitance C_{TOT} between V_S and V_+?
   b. What is the charge on the top plate of that capacitance?

   Now assume that S_1 and S_c are opened, all bottom plate switches are switched to V_{SS}=GND, except the switch on 16C which is switched to V_{REF}.
   c. What is the total capacitance C_1 between VREF and V+?
   d. What is the total capacitance C_2 between GND and V+?
   e. What is the voltage on V+ (in terms of VS and VREF)?

   Now assume that a value $B=b_4b_3b_2b_1b_0$ (a number between 0 and 31) is applied to the bottom plate switches, where b_i=1 means that the switch is on V_{REF}, and b_i=0 means that the switch is on GND.
   f. What is the total capacitance C_1 between V_{REF} and V+?
   g. What is the total capacitance C_2 between GND and V+?
   h. What is the voltage on V+ (in terms of VS and VREF)?
   i. Now assume an input voltage V_S=0.6V, V_{REF}=1V, and draw the voltage on V+ in each of the different clock phases assuming a SAR loads the analog value during the first clock period, and then switches each of the bits b_i in subsequent periods based on the signal from the comparator. You should get something along the lines of what is done on slide 10, which is conceptually what is going on, but not actually what the voltages will be (or the right number of bits).
2. In a particular process, long channel (1um) devices can be very roughly modeled as quadratic with μ_nC_{ox}=200uA/V2, μ_pC_{ox}=100uA/V^2, V_{tn}=0.3, V_{tp}=-0.3, $\lambda_n=\lambda_p$=1/(10V). If you have a 100nF capacitor that starts with a voltage of 1V, and a switch to ground implemented as an NMOS transistor with W/L=10u/1um
   a. Carefully sketch I_d vs V_{ds}=0..1 for the transistor with Vgs=0.4V.
   b. What is the "on resistance" R_{on} of the MOSFET?
   c. Assuming that the gate voltage of the NMOS devices rises from 0 to 0.4V at t=0,
      i. carefully sketch the capacitor voltage vs. time, clearly showing the shape for when V_C>0.1V, and the time that it takes to reach 0.1V.
      ii. What is an upper bound on the time that it takes for VC to fall from 0.1V to 5% of that value, 5mV (hint: think $2R_{on}$)
      iii. The sum of these times is roughly the time required to settle to 0.4% accuracy when starting with a large voltage. What is that sum?
3. A PMOS-input folded cascode with a supply from 0 to V_{DDA} in unity gain feedback has its positive input driven from 1V to ground. With only a capacitive load, what is the initial rate of change of the output voltage? What is the first device to drop out of saturation? Estimate the output voltage after the amplifier has settled.
4. You add a PMOS-input common source amplifier as a second stage to the output of the amplifier in the previous problem (and stabilize with a Miller capacitor!). With only a capacitive load, estimate the output voltage after the amplifier has settled, and the time to get within 0.1% of that value. (Hint: problem 2?)
5. An NMOS transistor is used as the ϕ_1 switch shorting out C_f in a PGA amplifier circuit similar to your project. Cf=10fF, and the NMOS device has a V_{tn}=0.5V, and C_{gd}=0.2fF.
   a. As ϕ_1 falls, what is the charge on C_{gd} just as the channel disappears (the switch opens, the device turns off, Vgs=Vtn)?
   b. After ϕ_1 goes to 0, all of that charge ends up on V-, and can not leave that node. During ϕ_2, where does it go (which capacitor, which side)?
   c. Assuming that Vin=0 during ϕ_1, what is the output voltage due to this charge injection?
6. A thin oxide NMOS transistor is used as the ϕ_2 switch shorting C_i to ground in the same PGA amplifier. When ϕ_2 is high, the gate oxide tunneling current density is 1A/cm2. The transistor is 1um/0.1um.
   a. What is the gate area, and the tunneling current through the gate to the drain?
   b. What is the rate of change of the output voltage due to the gate leakage (tunneling) current?
   c. How much does the output voltage fall in 5us?

7. To model the negative voltage spike on V- in the PGA, assume that the op-amp is very slow and its output stays at ground while an ideal ϕ_2 switch closes. Assume that C_f=100fF now.
    a. If V_{in}=1V, and gain=1, what is the voltage on V- just after ϕ_2 goes high?
    b. If V_{in}=1/8 V, and gain=8, what is the voltage on V- just after ϕ_2 goes high?
    c. If V- = -0.5V, draw a cross section of the ϕ_1 switch, label the voltages just after ϕ_2 goes high, and show which diode is forward biased. When current flows in that diode, does the output voltage end up higher or lower than it should be (after settling)?
    d. Now assume that the ϕ_2 switch has a series resistance of 10kΩ, and calculate the RC time constant of the ϕ_2 switch effect on V-
    e. If your op-amp has a unity-gain frequency of 20 Mrad/s, what series resistance should you choose for your ϕ_2 switch to match the op-amp and RC time constants?

Other stuff that might be interesting but won't be on the exam:

1. Take a look at the datasheet for the TI MSP430FG439 embedded microprocessor.
http://www.ti.com/lit/ds/symlink/msp430fg439.pdf
    a. Section 5.25 has the timing specs for the ADC. What is the typical clock frequency and max conversion time with the internal oscillator? How many cycles of the internal oscillator are required to convert an analog voltage to digital, and how does that compare to the number of bits?
    b. Section 5.26 has the linearity specs of this nominally 12 bit SAR ADC. Given the typical and max total unadjusted error, what is the actual number of ADC bits that you can trust?
    c. Section 5.27 has the specs for the built in temperature sensor. What is the typical voltage at 0C? What is the expected voltage at 25C (use TC_{sensor})? What is the chip-to-chip variation in the temperature sensor voltage (see note 2)
2. Take a look at the User's Guide for the same part
http://www.ti.com/lit/ug/slau056l/slau056l.pdf
    There are a lot of analog MUXes in Figure 22-1 for selecting how analog signals are routed to, from, and around the programmable gain op-amp. Figure out how to set all of the lower-right switches and MUXes to get a closed-loop gain of 2 from this system.