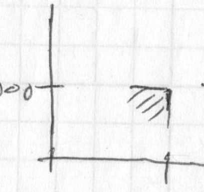
Midterm next Friday — 1 page notes, 2 sides, no calculators, cell phones, ...

HW3 v2 - fixed

CMOS inverter

Specifications $\Rightarrow$ freq response $\Rightarrow$ amp parameters G_m, R_o $\Downarrow$ circuit & device design

"gain of at least 1,000 at 20 kHz" $\longrightarrow$



"$\geq 1V$ output swing"

"with a 1pF load"

W, L

I_D (bias point)

V_{dsat}

lots of trade offs: Design!

$A_{vo}, \omega_p, \omega_u \Longleftrightarrow G_m, R_o, C_L \Longleftrightarrow g_m, r_o, C_{gs}, C_{gd}$

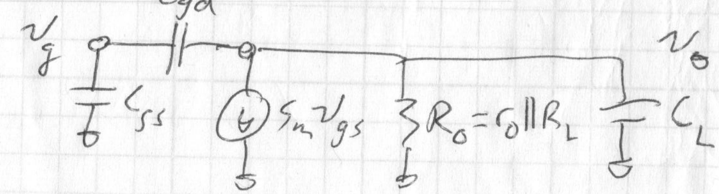
last time

$\frac{W}{L} = \frac{4\mu}{1\mu}$ vs. $\frac{W}{L} = \frac{400\mu}{1\mu}$

$V_{ov} = 1V \longrightarrow V_{ov} = 0.1V$

smaller V_{ov} @ const current

$\longrightarrow$ bigger gain, wider BW



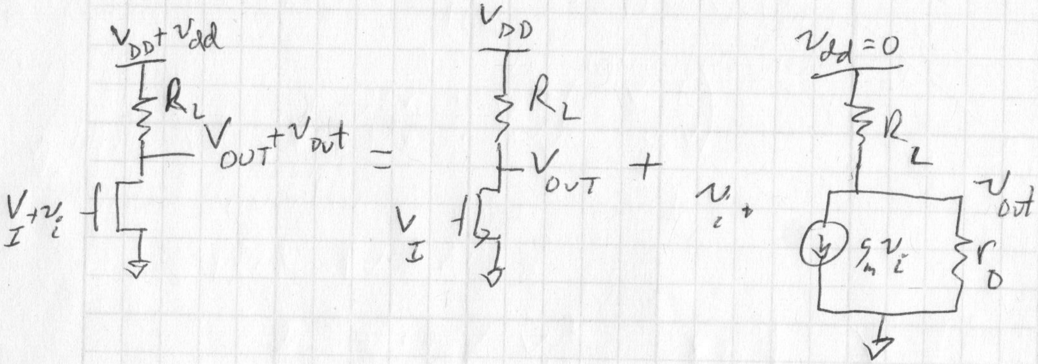
low freq: driving R_o: $-g_m R_L$

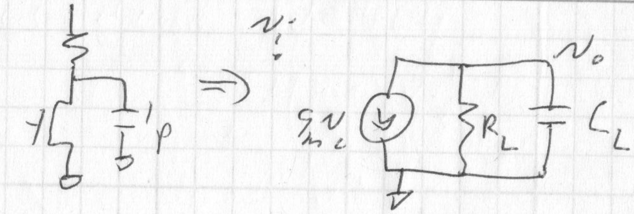
high freq: driving C_L: $\frac{-g_m}{j\omega C_L}$

highest freq: C_{gd} driving C_L: $\frac{C_{gd}}{C_{gd}+C_{gs}}$

linearize

bias point



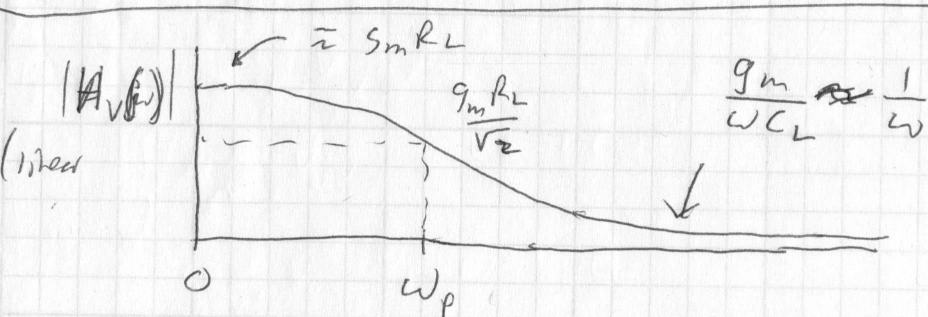


KCL @ v_o $\quad g_m v_i + \frac{1}{R_L} v_o + sC_L v_o = 0$

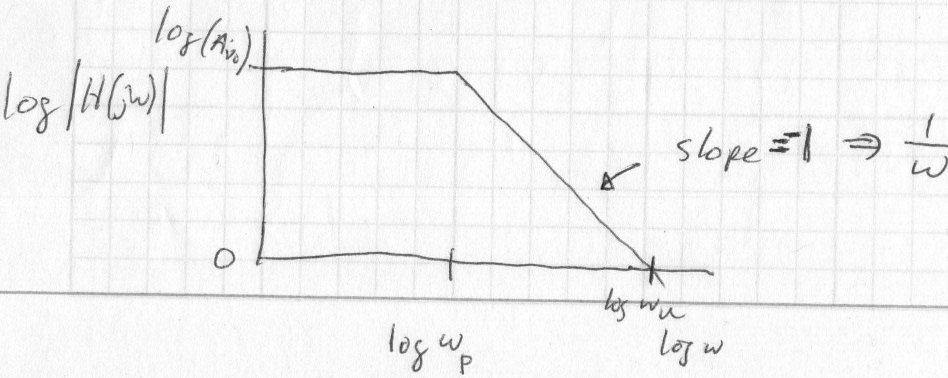
$$\Rightarrow \frac{v_o}{v_i} = \frac{-g_m R_L}{1 + sR_LC_L} = \frac{A_{vo}}{1 + s/\omega_p}$$

$|A_{vo}| = g_m R_L$

$\omega_p = \frac{1}{R_L C_L} \qquad \omega_u \equiv \frac{g_m}{C_L}$

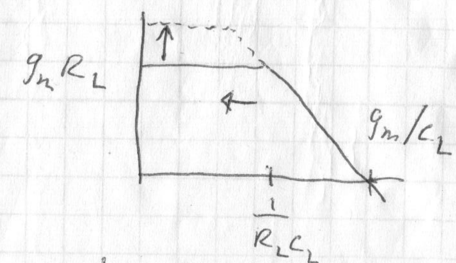


linear scale not so useful



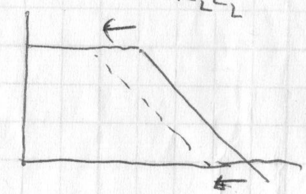
effect of increasing R_L

$A_{vo}\nearrow \; \omega_p \searrow$



increasing C_L

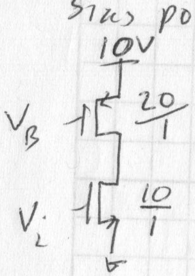
$\omega_p \searrow \; \omega_u \searrow$



increasing g_m

$A_{vo}\nearrow \; \omega_u \nearrow$

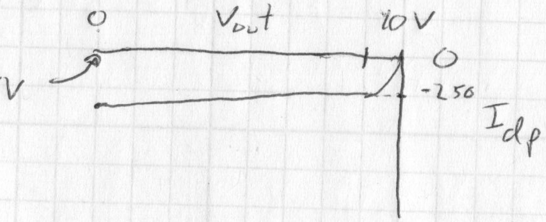
Bias point



$\mu_n C_{ox} = 50 \frac{\mu A}{V^2}$ $\mu_p C_{ox} = 25 \frac{\mu A}{V^2}$

$\lambda = 0.05\, V^{-1}$ $V_{DD} = 10V$

$|V_T| = 2V$



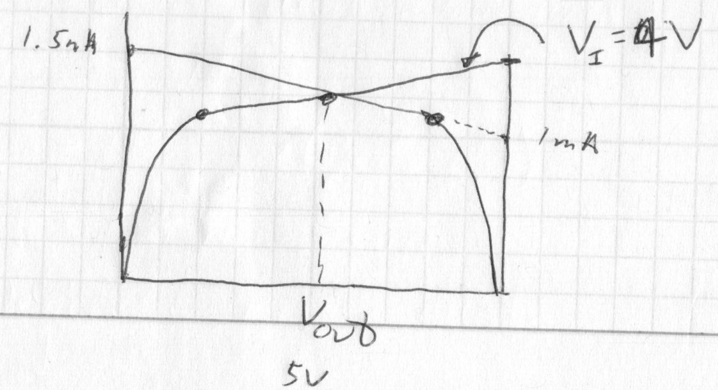
$V_B = 7V$ $-I_{dp} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_p \left(V_{GS} - V_{tp}\right)^2 (1 + \lambda V_{DS})$

what V_I do we need if $V_B = 6V$?

$I_{DN} = \frac{\mu_n C_{ox}}{2} V_{OV}^2 (1 + \lambda V_{DS}) = 250 \frac{\mu A}{V^2} V_{OV}^2 \left(1 + \frac{V_{DS}}{20V}\right)$

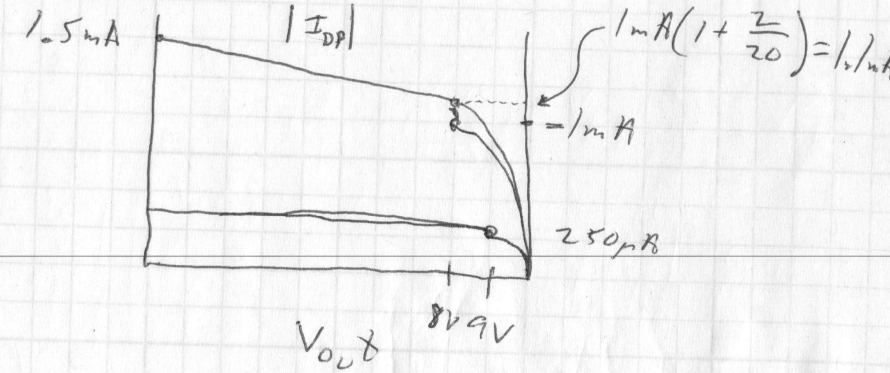
pick $V_{OV} = 2V \Rightarrow V_{GS} = 4V$

$I_{DN} = 1mA\left(1 + \frac{V_{DS}}{20V}\right)$



$|I_{DP}| = \left(250 \frac{\mu A}{V^2}\right)(-1V)^2 \left(1 + 0.05 \frac{1}{V} |(V_{out} - 10V)|\right)$

$= 250\mu A \left(1 + \frac{|V_{DS}|}{20}\right)$



Upper limit of PMOS saturation

$I_{DN} = \cancel{1mA\left(1 + \frac{8V}{20V}\right) V_{OV}^2 = 1mA}$

$= 250 \frac{\mu A}{V^2} V_{OVn}^2 \left(1 + \frac{8V}{20V}\right) = 1.1mA = I_{DP}$

$V_{OV} = \sqrt{\frac{1.1mA}{0.25 \frac{mA}{V^2}(1.4)}} = 1.77V,\ V_I = 3.77$

Lower limit $I_{DN} = 250 \frac{\mu A}{V^2} V_{OVn}^2 \left(1 + \frac{2V}{20V}\right) = 1mA\left(1 + \frac{8V}{20V}\right)$

$V_{OV} = \sqrt{\frac{1.4mA}{\left(0.25 \frac{mA}{V^2}\right)(1.1)}} = 2.26,\ V_I = 4.26$

$A_V = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{8 - 2V}{3.77 - 4.26} = -12$