Project

ADC clock edges

Signups this week
RRR week

electronic turn-in

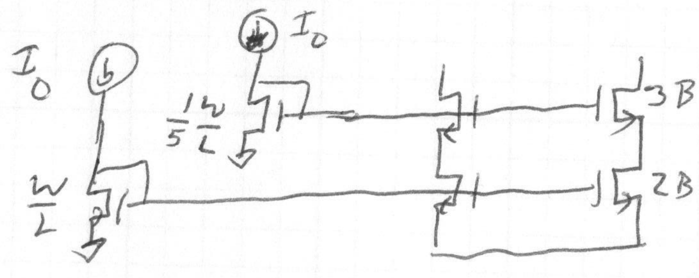
Extra OH

High-swing cascode bias

DREG

speed vs. L

compare to NMOS biasing



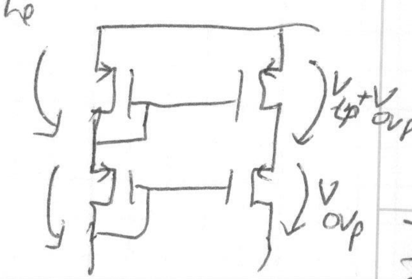
the source of M3B is just over V_{ov2B} above ground.

Much better swing.

High swing cascode biasing

Problem: diode connected cascodes cause headroom headache

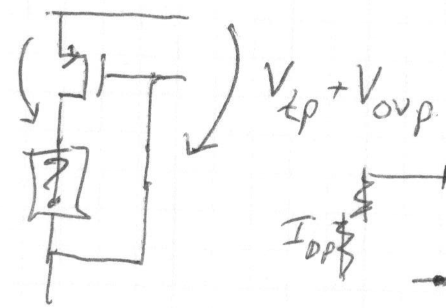
$\approx 1V \left\{ \begin{array}{l} V_{tp}+V_{ovp} \\ V_{tp}+V_{ovp} \end{array} \right.$

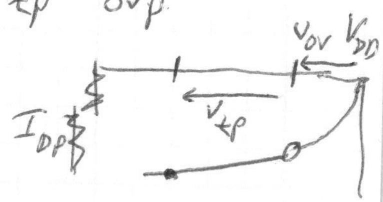


the source of M4A is stuck at $V_{tp}+V_{ovp}$ away from V_{DD}

Can we do the same w/ ~~PMOS~~ mirrors?

Consider





What could go in the box?

Resistor

Battery

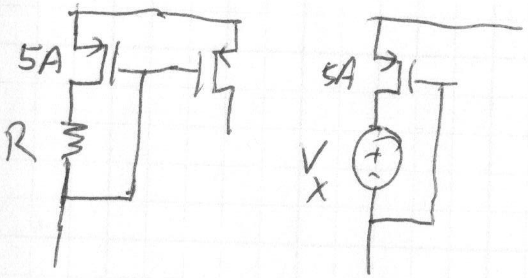
Diode

~~Dio~~ Anything that lets current $\underline{\text{down}}$ with less than V_{tp} voltage drop

140

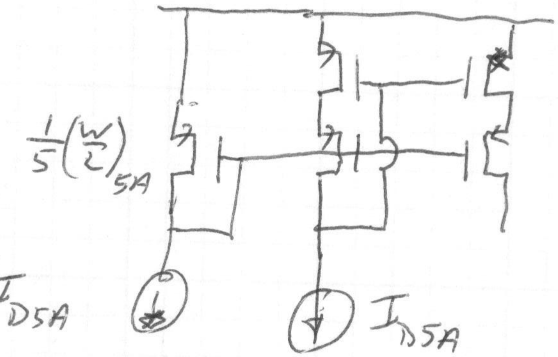
16sp

W14L7

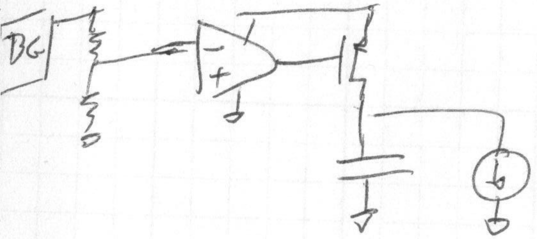


Q: How big can R or V_x be and still have 5A in saturation?

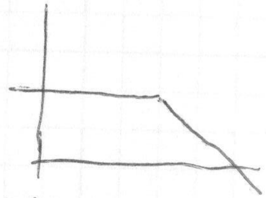
A: $I_{D5A} R < V_{tp}$ $\quad V_x < |V_{tp}|$



Digital REG



2nd stage



relatively low gain

relatively low freq pole

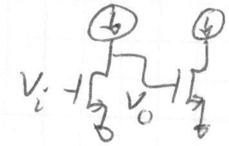
need either

op-amp phase contributions

$\rightarrow \underbrace{\omega_{p2}\, A_{v1} A_{v2}}_{W_{u2} A_{v2}}$

or put op-amp pole at very low freq, some pole splitting

Speed



unity gain frequency for a transistor driving a copy of itself.

$A_v = g_m r_o$

$\omega_p = \frac{1}{r_o C_{gs}}$

$\omega_u = \frac{g_m}{C_{gs}}$

$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$

$C_{gs} = \frac{2}{3} W L C_{ox}$

$\omega_u = \frac{3\mu_n}{2} \frac{V_{ov}}{L^2} = \frac{3}{2} \mu_n \underbrace{\frac{V_{ov}}{L}}_{E} \frac{1}{L}$

velocity

$\approx \frac{1}{\tau}$ $\quad \tau$: transit time $= \frac{L}{\text{velocity}}$

In scattering limited case

$I_D = W C_{ox} v_{scl} V_{ov}$

$g_m = W C_{ox} v_{scl}$

$\omega_u = \frac{g_m}{C_{gs}} = \frac{W C_{ox} v_{scl}}{\frac{2}{3} W L C_{ox}} = \frac{3}{2} \underbrace{\frac{v_{scl}}{L}}_{\frac{1}{\tau}}$

ω_T = transit frequency