Project

Final Design due < 2 weeks (9 AM Monday)

presentations on going: David, me, next wk 14,

RRR I designed, I calculated, I measured

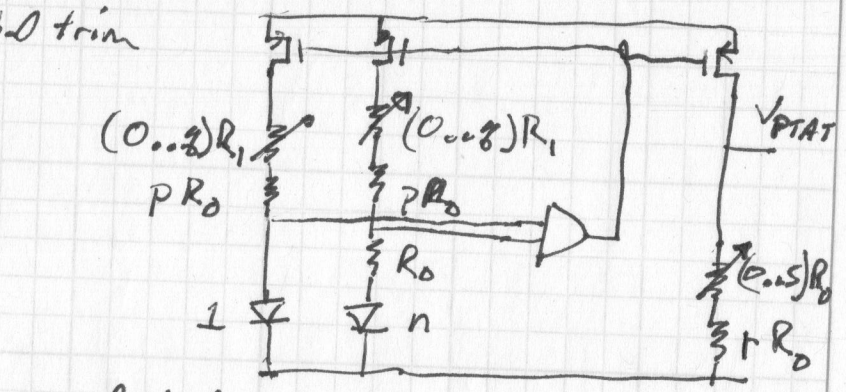
Wafer sort - die-level testing of chips

- acceptance testing, binning, BIST
- digital trimming

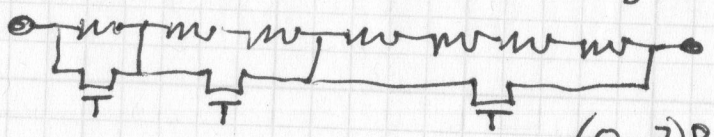
Charge injection

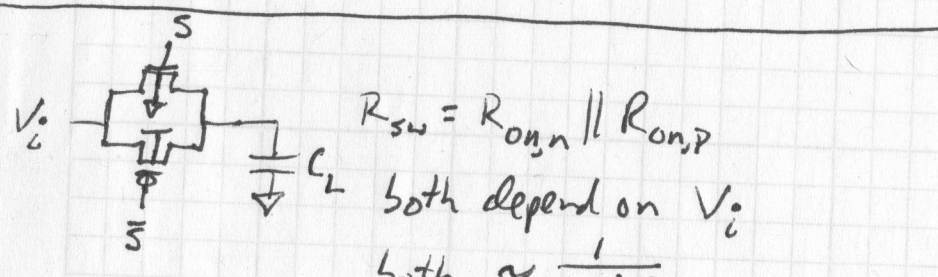
Settling

Digital trim



pR_0 < desired < ~~$(p+7)R_0$~~ $pR_0 + 7R_1$



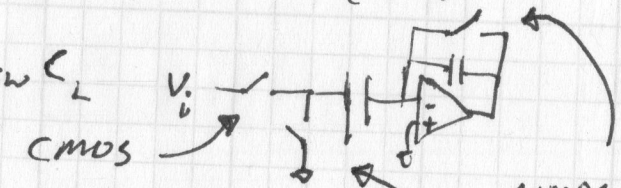


$R_{sw} = R_{on,n} \parallel R_{on,p}$

both depend on V_i

both $\sim \frac{1}{(W/L)}$

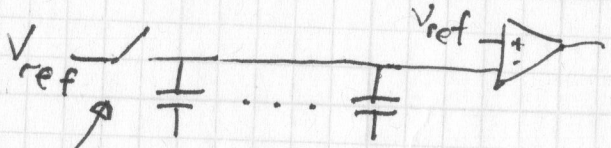
$\tau = R_{sw} C_L$



minimum sized NMOS

$W/L = 130nm/65nm$

~ 5K pull down (to ground)



Big capacitor $2^8 C_{min} = 2.56\,pF$

Minimum sized PMOS $R_{on} = 50K$?

$\tau = 100ns$?

maybe OK

if not, need to make W wider

problem: charge injection as switch turns off

After settling $V_o = V_i$ $I_D = 0$ $Q_{ch} = C_{ox}(V - V_i - V_t)$

$Q_{ch} = C_{gs}(V_{GS} - V_t) = WLC_{ox}(V_{DDA} - V_i - V_t)$

e.g. $(0.13\mu)(0.065\mu)\left(10\frac{fF}{\mu m^2}\right)(1.2 - 0 - 0.3)$

$\simeq (0.1fF)(0.9V) \sim 0.1fC$

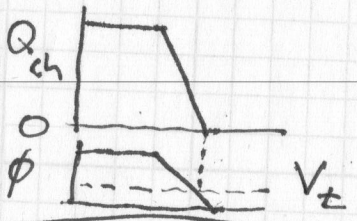
where does the charge go?

fast clock: ϕ falls faster than τ

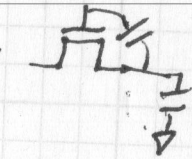
$\Rightarrow \frac{1}{2}$ goes to source, $\frac{1}{2}$ to drain

ΔQ injected $= \frac{1}{2} WLC_{ox}(V_{DDA} - V_i - V_t)$

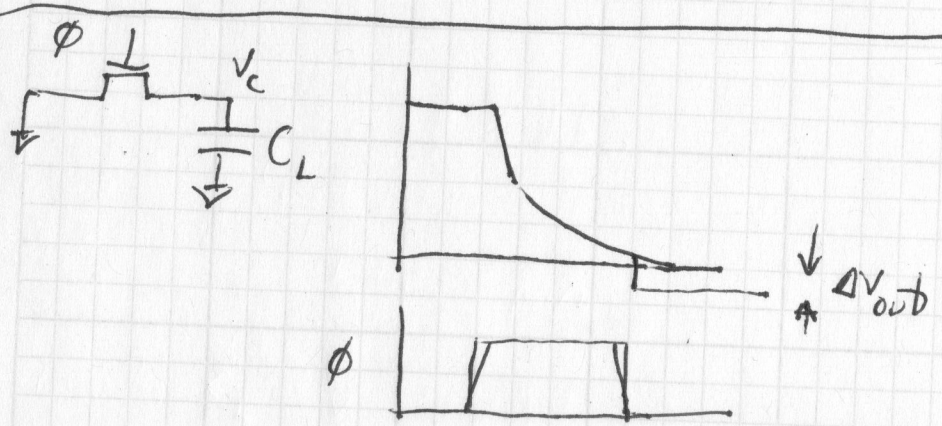
slow clock: all channel charge bleeds off



what about C_{gd}?



$Q_{gd} \geq V_t C_{gd}$



$\Delta V_{out} = \frac{\Delta Q}{C_L} \geq \frac{V_t C_{gd}}{C_L}$ e.g. $(0.5V)\frac{1fF}{10fF}$

$= 50mV$