Project

- Signups for intro presn : team intro
  block diagram + assignments
  Lab 4/5 results (some)
  Questions +

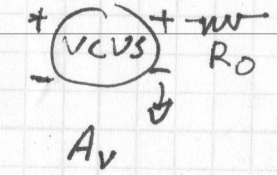
HW9 opamps - resistive load ⇒ 2 stage!

gate leakage real world: thick oxide devices for I/O
140: turn it off!

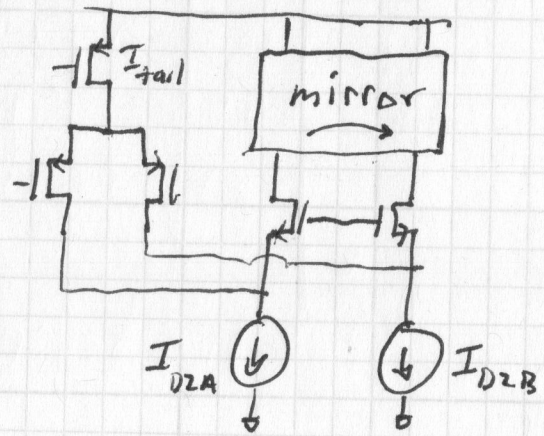
Results when you get something that you like
- name it
- save a copy e.g. PGAapril12
- include a schematic in your ppt

Don't edit the named copy!

Debugging - start w/ ideal amps and make them more real
- try to not ignore the things you don't understand



Folded Cascode Biasing & Freq response



$I_{D\,3,4,5} \simeq I_{D2A} - \frac{1}{2} I_{tail}$

If $I_{D2} \simeq I_{TAIL}$ then 1, 3, 4, 5 all have roughly the same currents.

Current mirror has same pole/zero as before (W9L2)

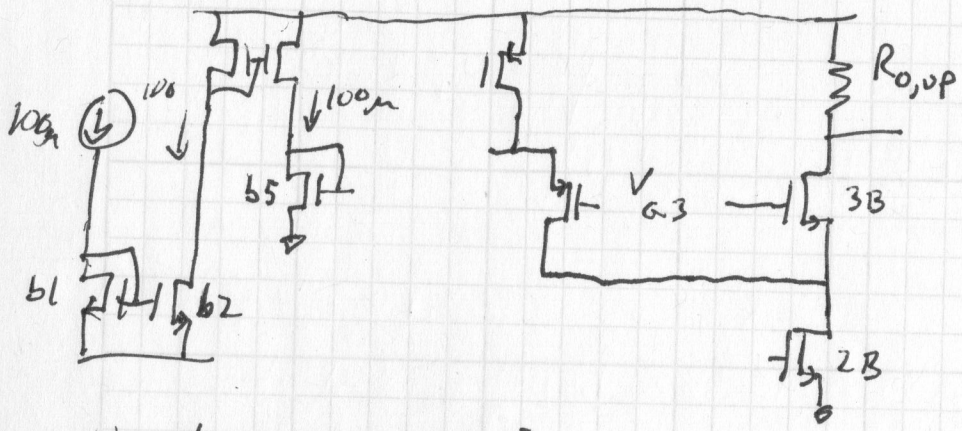
$$\omega_{pm} = \frac{g_{m5}}{2C_{gs5}}$$

$$G_m = -g_{m1B}\frac{v_{id}}{2} - g_{m1A}\frac{v_{id}}{2}\left(\frac{1}{1+s/\omega_{pm}}\right)$$

$$= -g_{m1}\frac{v_{id}}{2}\,\frac{2+s/\omega_{pm}}{1+s/\omega_{pm}}$$

$$= -g_{m1}v_{id}\,\frac{1+s/\omega_{zm}}{1+s/\omega_{pm}}$$

$$\omega_{zm} = 2\omega_{pm}$$



How to size Mb5?

What is $V_{G3,min}$?

$V_{D2B,min} = V_{OV2}$

$V_{G3,min} = V_{OV2} + V_{tn} + V_{OV3} = V_{tn} + 2V_{OV}$

Assuming $I_{Db5} = I_{Db1}$ & Len

$$\left(\frac{W}{L}\right)_{b5} V_{OV,b5}^2 = \left(\frac{W}{L}\right)_{b1} V_{OV,b1}^2$$

$$V_{OVb5} = \sqrt{\frac{(W/L)_{b1}}{(W/L)_{b5}}}\, V_{OV,b1}$$

Theoretically: $\left(\frac{W}{L}\right)_{b5} = \frac{1}{4}\left(\frac{W}{L}\right)_{b1}$

$$\Rightarrow V_{OVb5} = 2\, V_{OV,b1}$$

better to play it safe and use at least 5:1

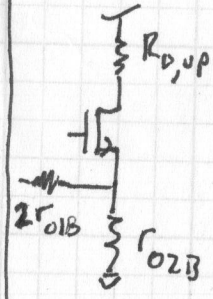
If <u>not</u> quadratic

- choose based on appropriate model
- verify w/ simulation

Poles at sources: most are low impedance $\sim \frac{1}{g_m}$

so high freq $\sim \frac{g_m}{2C_{gs}}$

source of M_{3B} ~~that~~ is high impedance at low freq.



Pole at 53B: when |impedance| of capacitance $= \frac{1}{\omega 2 C_{gs3}}$

is equal to the impedance "looking up"