EE140: Lab 3

2 stage bipolar op-amp

Due: Week 8, 2016

Instruction

For this lab, you may consult the professor, the TAs, your friends, the textbook, the internet, and any other living or inanimate objects, with the exception of your peers' lab reports. You may obtain data in pairs, but must **submit your own written report**. Be concise. Hand calculations should be to 1 or at most 2 digits of precision. Don't use a calculator – I won't let you use one on the exam and it's good to get in practice.

Objective

This lab is meant to familiarize you with 2-stage op-amps, and in particular unity-gain feedback.

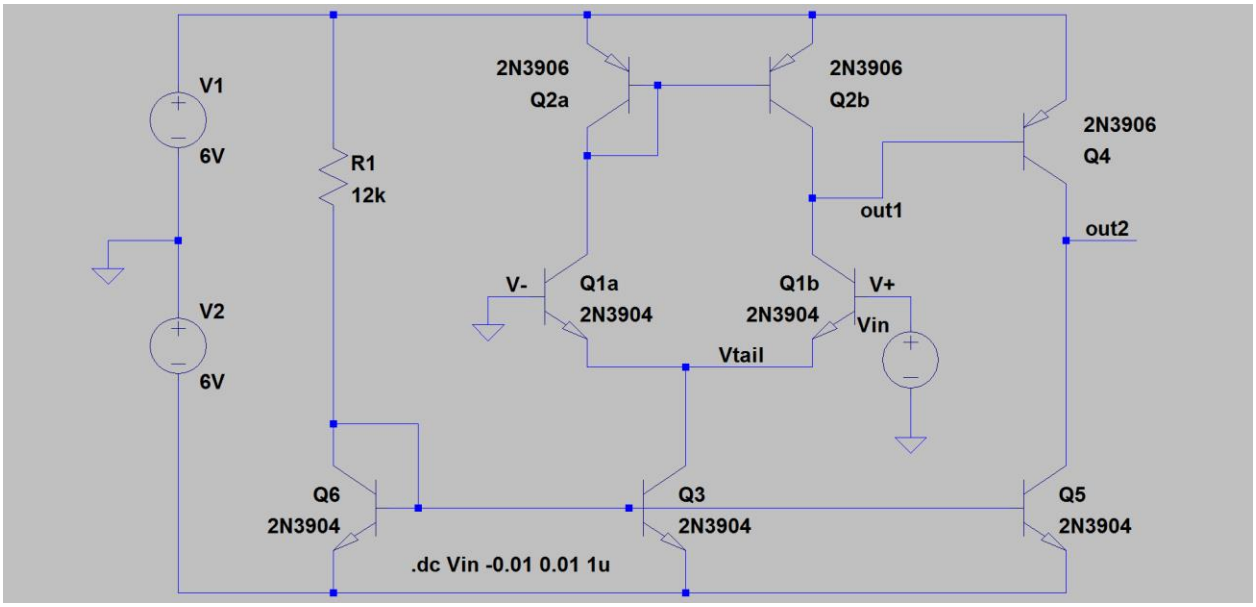

Figure 1: Lab 2 Op-Amp [File: BJTopamp.asc]

SPICE model parameters. You can see the parameters that LTSPICE uses by right clicking on an element and selecting "Choose new device". The parameters that you need for your hand analysis are:
2N3904 NPN (VAF=100 Bf=300 CJC=4p CJE=8p)
2N3906 PNP (VAF=100 Bf=200 CJC=5p CJE=10p)
PRELAB – Hand analysis and SPICE

1. [Writeup] Hand calculate, for Vin=0, the following values. 1 sig-fig is fine (i.e., I_{C6}=1mA is close enough)
    a. all bias currents and bias voltages. Make a table with columns for transistors and rows for the various parameters.
    b. g_m and r_o for all devices, and $r_{\pi 4} = \beta/g_{m4}$ for Q4

c. the DC gain from Vin to out1 **without** the 2nd stage connected.
d. the DC gain from Vin to out1 **with** the 2nd stage connected. This is one case where we see an important difference between bipolar and MOS. The small signal input resistance of Q4, $r_{\pi 4} = \beta/g_{m4}$, is the smallest resistance at node out1, and substantially lowers the DC gain of the first stage.
e. the DC gain from out1 to out2, and from Vin to out2.

2. Use LTspice on the file BJTopamp.asc to run a DC sweep on the amplifier in Figure 1.
   a. Click on the out1 wire. Find the highest gain from Vin to out1.
   b. Click on the out2 wire. Find the highest gain from Vin to out2, and over that region of highest gain, calculate the gain from out1 to out2.
   c. [Writeup] Compare your hand calculated gains to the gains that you measured in 2a and 2b.

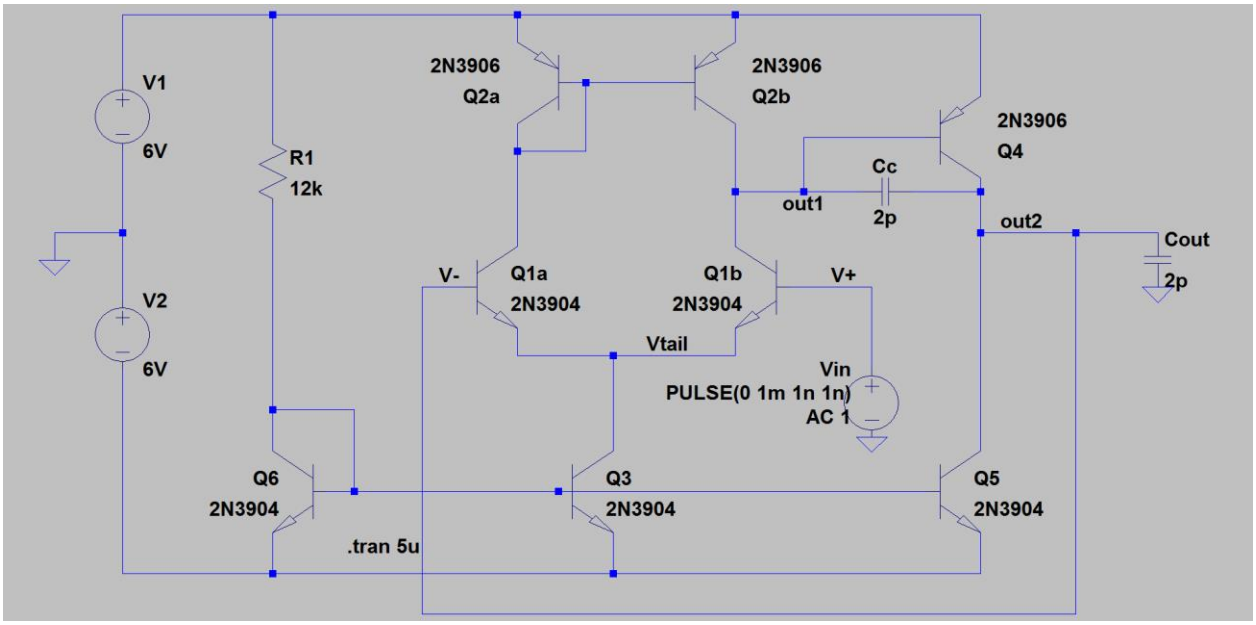

Figure 2. The op-amp in unity gain feedback. Capacitors Cc and Cout represent typical parasitics for a breadboard.

3. Use LTspice on the file BJTopampUnityFB.asc to simulate the amplifier in unity gain feedback, as shown in Figure 2. This amplifier is unstable in unity-gain feedback.
   a. [Writeup] The input is a 1mV step. What should the output be?
   b. Use the cursor tool to measure the frequency of the fully-developed oscillation (where the amplitude is roughly 300mV peak-to-peak).
   c. Use the cursors to measure the period of the first several oscillations (when the amplitude grows from 0 to ~200mV peak-to-peak).
   d. [Writeup] How does the frequency of oscillation change as the amplitude of the oscillation increases?
   e. Use the cursors to measure the amplitude of each half cycle (peak-to-trough, trough-to-peak) of the oscillation during the first several oscillations. Plot using excel or other tool. You should see an exponential growth.
   f. [Writeup] Estimate the location of the complex conjugate poles of the closed-loop amplifier, and how they move as the output rings up.
4. We now want to stabilize the amplifier by moving the poles around.

a. Increase Cout to 1000pF. Measure the negative slew rate.
b. [Writeup] Estimate the negative slew rate assuming Q4 is off. What is the amplifier doing that allows the positive-going rate of change to be so much larger than the negative?
c. Increase Cout to 20,000pF=20nF. Estimate the closed-loop pole locations. Is the amplifier settling to the right value?
d. Increase Cout to 200,000pF=200nF. Estimate the closed-loop pole locations.
e. Increase Cout to 1,000,000pF=1uF. What is the settling time (time to get within 5% of the final value)?

Now set **Cout back to 2pF**, and we'll try using Cc instead.

f. Set Cc=100pF. Estimate the closed-loop pole locations.
g. Set Cc=600pF. What is the settling time?
h. [Writeup] Compare the size of the capacitor needed to stabilize the amplifier, and the resulting settling times.
i. Change the input step to be 1000mV instead of 1mV. What is the slew rate?
j. Change the input step to be -1000mV. What is the slew rate?
k. [Writeup] Compare these slew rates to hand calculated slew rates, and in each case describe which transistors are off, and which are carrying I_{tail}.
l. **Set Cc=2pF**, and add a capacitor C_1 from out1 to ground. What value of C_1 is needed make the amplifier stable in unity gain feedback?

5. And finally, we can show that even without compensation capacitors the amplifier is stable when the feedback factor is small enough. Run the simulation for BJTopamp100xFB.asc, and note that it is stable even with Cc=Cout=2pF. What is the feedback factor and gain in this case?

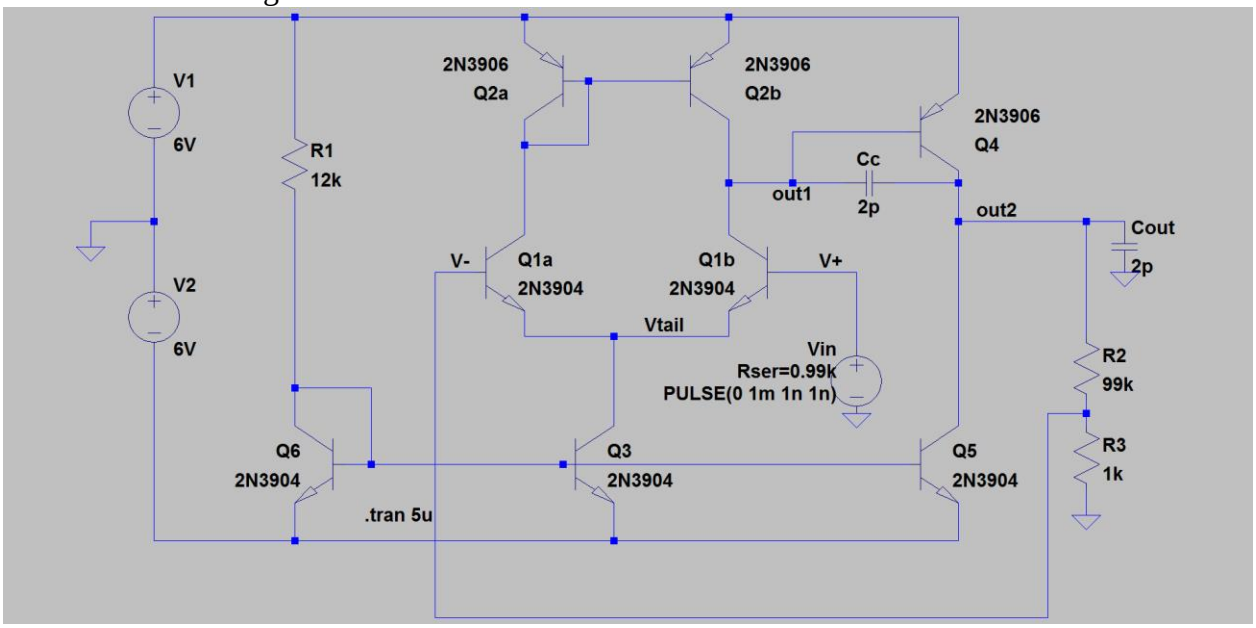

Figure 3: Note that I changed Vin to have a source resistance of 0.99k to match the feedback network, to avoid the effect of input bias current. Not necessary in CMOS.

Lab

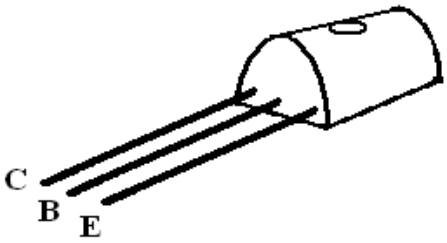

Figure 2: BJT Pin Configuration

1. Build the circuit in *Figure 1* .

2. Measurements
    a. DC Biases
        i. Ground Vin and measure the tail voltage, the base voltage of Q6, and the base voltage of the Q2 mirror. Make sure that they are consistent with your hand calculations, and simulations.
        ii. Debugging tip: always start by checking that your supplies are where you think they are. Measure from ground to each supply, and from the bottom to the top. The gains in this amplifier are so high that it is quite likely that out1 and out2 will not be exactly where you expect.
    b. Keep the negative input grounded, and sweep the positive input near 0V. Try to measure the gains. This is hard, because they are so large. Try to be clever – if your input is a slow ramp, and you know the rate of change, can you use that to figure out the gain? Verify that out2 swings nearly rail to rail.
        i. Take a picture of the results. Compare to the spice plot and comment on any differences.
        ii. Show both of these to your TA. TA initials_____
    c. Put the amplifier in unity-gain feedback, and drive the input with a small square wave at low frequency. Watch it ring. Take a picture.
    d. Add capacitance at the output. Can you replicate the behaviors that you saw in the simulation (saw tooth, stable but ringing, stable and no overshoot)? What is the best settling time you can get? Take a picture of each behavior, and note the corresponding capacitance.
    e. Remove the capacitance at the output, and add capacitance across the second stage (C_c). Can you replicate the behaviors that you saw in the simulation (stable but ringing, stable and no overshoot)? What is the best settling time you can get? Take a picture of each behavior, and note the corresponding capacitance.
    f. [Writeup] Compare the amount of capacitance used at Cout and Cc, and its effect on the closed-loop step response.