

A Differential Switched-Capacitor Amplifier with Programmable Gain and Output Offset Voltage

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ABSTRACT

The design of a low-power differential switched-capacitor amplifier for processing a fully-differential input signal coming from a pressure sensor interface is reported. The circuit is intended to amplify the input signal, convert it to single-ended mode and shift its output by an offset voltage. The gain and output offset voltage are digitally programmable. The differential switched-capacitor amplifier employs an op amp voltage cancellation technique without requiring its output to slew to analog ground each time the amplifier is reset. Additionally, the circuit topology is very insensitive to low op amp gain and allows to attain 9-bit linearity. Moreover, a switched-capacitor common-mode feedback configuration with symmetric loading of the differential mode loop has been adopted to reduce charge injection and leakage current errors as well as to settle much faster than traditional CMFB circuits. The circuit has been successfully integrated into a SoC device where, after the analog pre-processing, the pressure sensor signal is measured through a 10-bit ADC. Implemented in a standard 4-metal single-poly 0.25 μ m CMOS process, the module occupies a silicon area of 0.115 mm², operates down to 1.8V and its 3-V typical current consumption is 40 μ A.

Categories and Subject Descriptors

B.7.m [Integrated Circuits]: Miscellaneous.

General Terms

Design, Performance, Experimentation.

Keywords

Analog integrated circuits, switched-capacitor filters.

1. INTRODUCTION

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The continuous increase in System-on-Chip (SoC) complexity has been placing strong constraints to analog Intellectual Proprietary (IP) design. Although SoCs are usually targeted to digital-tailored technologies for financial reasons, they frequently demand low-power low-voltage high-accuracy analog IPs. One way to overcome these conflicting requirements is the use of Switched-Capacitor (SC) circuits. Switched-capacitor technique efficiently compensates input offset and finite gain errors inherent to operational amplifiers (op amps). Moreover, due to its purely capacitive load, op amps do not require a high-power output driver, reducing area and power consumption as well as greatly simplifying frequency compensation as the load capacitance itself compensates the op amp. Finally, high accuracy and programmability are achieved with careful design and layout of capacitor ratios.

The circuit presented herein is a low-power switched-capacitor amplifier implemented with metal (MiM) capacitors to achieve high linearity and device matching. Its architecture is described in Section 2 while Section 3 addresses its main design considerations. Experimental results are summarized in Section 4 followed by the final conclusions in Section 5.

2. CIRCUIT DESCRIPTION

Fig. 1 illustrates a block diagram of the Differential Amplifier (DA). It is composed by 2 stages. First stage amplifies the differential input signal by 16 allowing $\pm 25\%$ of digital trimming. The second stage is a differential-to-single-ended, unity gain stage that adjusts the DC output level by adding an offset voltage programmable within $\pm 25\%$ using 2 trimming bits. Both gain and offset trimming add active calibration capability to the Differential Amplifier through the 10-bit Analog-to-Digital Converter (ADC). Hence any deviations in gain and offset can be stored in internal SoC registers for later software compensation. The Differential Amplifier control signals (clock, enable, test enable and ADC trigger) properly synchronizes the circuit with the pressure sensor and the AD converter.

The DA amplifies the input signal and adds an offset voltage to the output. Both gain and offset are functions of capacitor ratios. The mathematical description of the output voltage (derived from Fig. 2 and Fig. 5) is given by:

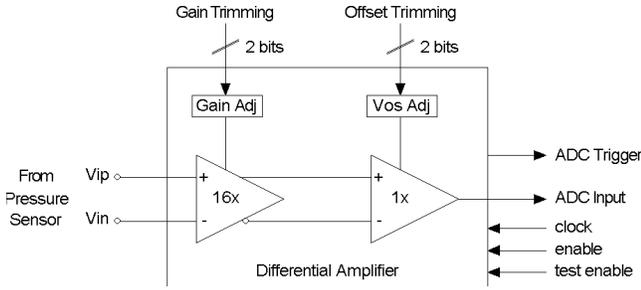


Figure 1. Differential Amplifier block diagram

$$V_o = \left(\frac{C_1}{C_2}\right) \cdot \left(\frac{C_4}{C_5}\right) \cdot (V_{ip} - V_{in}) + \left(\frac{1}{2} - \frac{C_7}{C_5}\right) \cdot (V_{DD} - V_{SS}) \quad (1)$$

where $(V_{ip} - V_{in})$ is the differential input voltage, V_{DD} and V_{SS} are the power supply voltages, $(C_1/C_2) \cdot (C_4/C_5)$ defines the amplifier gain and the term $[1/2 - (C_7/C_5)]$ corresponds to the DC level shift at the output. The pressure sensor can be modeled as a resistive Wheatstone bridge with a differential output signal ratiometric to $(V_{DD} - V_{SS})$. Also, the ADC voltage reference is ratiometric to $(V_{DD} - V_{SS})$. Therefore the DC level shifting at DA's output is proportional to the power supplies as well (nominally 600mV when $V_{DD} = 3V$ and $V_{SS} = 0V$). Both gain and offset capacitor array ratios can be adjusted by $\pm 25\%$ around 16 and 0.2, respectively, during calibration process. Each DA stage compensates for op amp gain and op amp offset errors. Also, first stage has a high immunity to virtual ground (or analog ground) variations thanks to its fully differential architecture.

The overall DA linearity is 9 bits (equivalent to the 10-bit ADC linearity). Due to its active calibration feature the Differential Amplifier gain accuracy has been set to 8 bits. However, noise floor in switches and capacitors is limited to 1/2 LSB within 10-bit resolution. In other words the DNL of the amplifying stage is 1/2 LSB at 10-bit resolution. Additional specifications of the circuit are: (a) power supply range from 2.1V to 3.6V; (b) input bandwidth of 100Hz; (c) DC input level at $V_{DD} = 3V$: $1.5V \pm 500mV$; (d) sampling frequency of $f_{clk} = 125KHz$; (e) temperature range from $-40^\circ C$ to $125^\circ C$; and (f) typical current consumption of 40uA.

3. CIRCUIT DESIGN

The switched-capacitor amplifier shown in Fig. 2 implements the gain stage cell and is the fully-differential counterpart of the amplifier presented in [1]. It is based on the Correlated Double Sampling (CDS) technique widely used to minimize errors due to finite offset voltages, 1/f noise, and finite op amp gain [2]. The CDS technique does not require a reset of the output in each clock phase, which alleviates the slew-rate requirements for the op amp. Also, as the non-ideal op amp effects are reduced, a more relaxed op amp specification for low frequency inputs can be attained.

The ground reference AGND comes from the analog ground generator and typically is $0.5 \cdot (V_{DD} - V_{SS})$. The classical feedback reset switch is replaced by the elementary sample-and-hold branches consisting of capacitors C_3 and their associated switches.

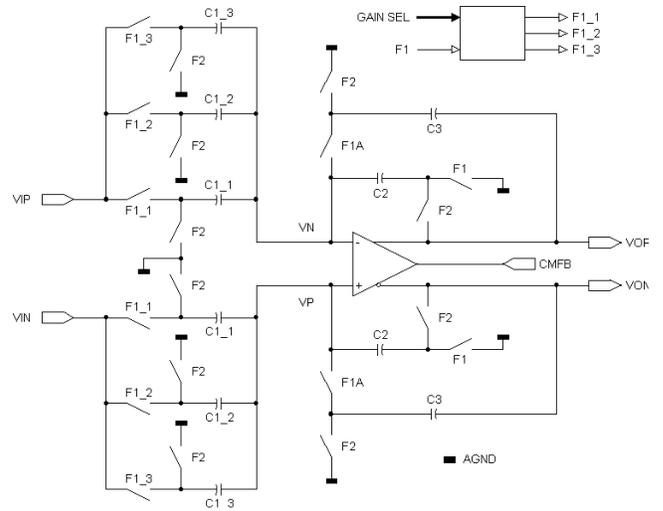


Figure 2. Gain stage cell

During amplification phase (F2), sampling capacitors C_1 discharge into C_2 and the valid differential output is generated. This output is stored in C_3 . In the sampling phase (F1), capacitors C_3 become the feedback capacitor while capacitors C_1 sample the difference among the input voltages and the voltages at the opamp inputs (vp and vn nodes). At the same time, any offset voltage will be differentially stored onto C_2 . In the next amplification phase, this offset voltage will be subtracted and cancelled.

As the input signal bandwidth is much smaller than half the sampling frequency, i.e., the signal is significantly oversampled, V_{op} and V_{on} do not vary much from one clock phase to the next. Thus, for a finite op amp gain (A_v), the signal voltage at the inputs of the op amp is a slowly varying signal which is therefore nearly cancelled by the CDS switching of C_1 and C_2 . This reduces the effect of finite op amp gain on the voltage gain of the stage. Detailed analysis of the fully-differential SC amplifier of Fig. 2 shows its DC gain is given by:

$$\frac{V_{op} - V_{on}}{V_{ip} - V_{in}} = \left(\frac{C_1}{C_2}\right) \cdot \left(1 + \frac{C_1 + C_2}{C_2 \cdot A_v \cdot (A_v + 1)}\right)^{-1} \quad (2)$$

Eq. 2 shows that the voltage gain does not depend on capacitors C_3 while the gain error is proportional to A_v^{-2} rather than A_v^{-1} . This feature allows us to adopt a moderate-gain ($\sim 70dB$) folded-cascade op amp without causing large errors in the amplifier gain. Besides reducing errors caused by op amp offset voltage and finite gain, the clock-feedthrough noise is also minimized by opening the switches connecting C_3 to the op amp inputs (phase F1A) slightly before than closing the switches connecting C_2 to analog ground (bottom plate sampling).

Trimming capability is accomplished dividing each sampling capacitor in 3 sets (C_{1-1} , C_{1-2} and C_{1-3}) of unit capacitors (C_u) as long as C_2 is also set to be equal to C_u . By default $C_{1-1} = 12C_u$ and $C_{1-2} = 4C_u$ define the sampling capacitor, so $(C_1/C_2) = 16$. By adding $C_{1-3} = 4C_u$ to the sampling capacitor, the amplifier gain becomes 20 whereas taking off C_{1-2} from the default value, the gain is set to 12.

The MiM capacitor size was initially estimated from maximum noise restriction but it provided a too small cap bound (1.45fF).

Being the DC amplifier gain determined by the capacitor ratio C_1/C_2 , a proper matching level is needed to achieve an overall linearity of 9 bits. Such matching level set a minimum capacitor size. From mismatch data for MiM capacitors in our CMOS process, it was estimated the minimum capacitor size to obtain a mismatch error of 0.0894% (equivalent to have an effective number of bits - ENOB - of 10.128 bits). So, for such a capacitor size, C_u was obtained. Additionally, to limit noise injection from the substrate, the plates of all the capacitors tied to the op amp inputs were maintained in the top metal mask.

The switch sizes were calculated based on the settling time error constraint. To get an error less than 0.5LSB for 10 bits, operating at a clock frequency of half clock frequency and taking into account a sampling capacitor of $16C_u$, the minimum switch resistor value obtained using hand calculations was 100KOhms. Then, it can be adopted devices with minimum geometries. Although, leakage imposes a channel length slightly higher than the minimum allowed.

Fig. 3 illustrates the schematic of the op amp. It is a fully-differential, folded-cascode, n-channel input transistors operational amplifier. One interesting feature about this opamp is its flexibility to be used either as a fully-differential or a single-ended amplifier. For single-ended applications, the inverted output terminal (OUTN) must be connected to the common-mode feedback input (CMC) which would normally be used by the common-mode feedback circuit to define the common-mode output voltage in fully-differential architectures. The use of low threshold voltage (V_{th}) transistors at the differential pair guarantees its operating voltage down to 1.7V. Typical electricals parameters for the op amp are 76dB open loop gain, 1.1MHz unit gain frequency with 69° phase margin, $11\mu A$ power consumption and output voltage swing ranging from $V_{DD} - 270mV$ to $V_{SS} + 230mV$.

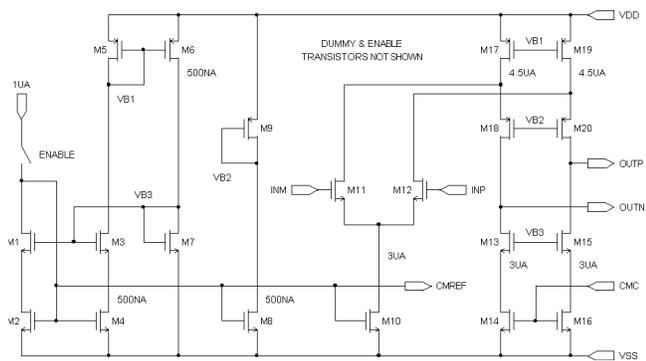


Figure 3. Schematic of the op amp

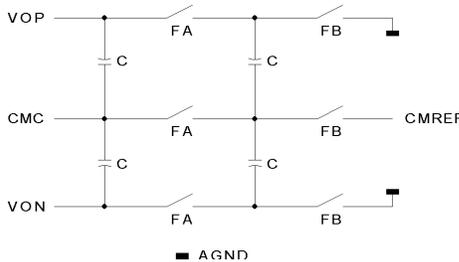


Figure 4. Schematic of the SC-CMFB circuit

The SC common-mode feedback (CMFB) circuit is shown in Fig. 4. It employs a switched-capacitor configuration with symmetric loading of the differential mode loop [3]. The symmetric loading is obtained doubling the circuit in Fig. 4 and exchanging the clock phases. This guarantees that both sampling and setting of the common-mode output are simultaneously performed at every clock phase. Therefore the op amp common-mode output settles much faster than (almost twice as fast as) using the traditional CMFB topology. To guarantee the CMFB circuit properly settles in PVT (process, voltage and temperature ranges), the Differential Amplifier starts working at half the clock frequency and, after 32 cycles ($512\mu s$), the clock is reduced to $f_{clk}/8$ to minimize op amp settling time errors.

After the common-mode feedback circuit stabilizes, a common-mode signal will appear at the inputs of the opamp. Note the common-mode signal is close to the analog ground plus the opamp offset voltage. However, that fact does not cause any harmful effects since the op amp common-mode rejection ratio is adequate (144dB typical). Further, parasitic capacitances at the op amp input terminals have not effect on the gain; the impact of other stray caps is diminished as long as they are well matched; careful layout addressed the demand of maintaining similar parasitic capacitance along all the differential paths.

Fig. 5 is the schematic of the differential to single-ended stage. It is based on the same SC CDS architecture adopted for the fully-differential amplifier stage but adapted to be a single-ended unity gain amplifier. Neglecting op amp finite gain and input offset errors, the transfer function of the second stage is given by:

$$V_o = \left(\frac{C_4}{C_5}\right) \cdot (V_{ip} - V_{in}) + \left(\frac{1}{2} - \frac{C_7}{C_5}\right) \cdot (V_{DD} - V_{SS}) \quad (3)$$

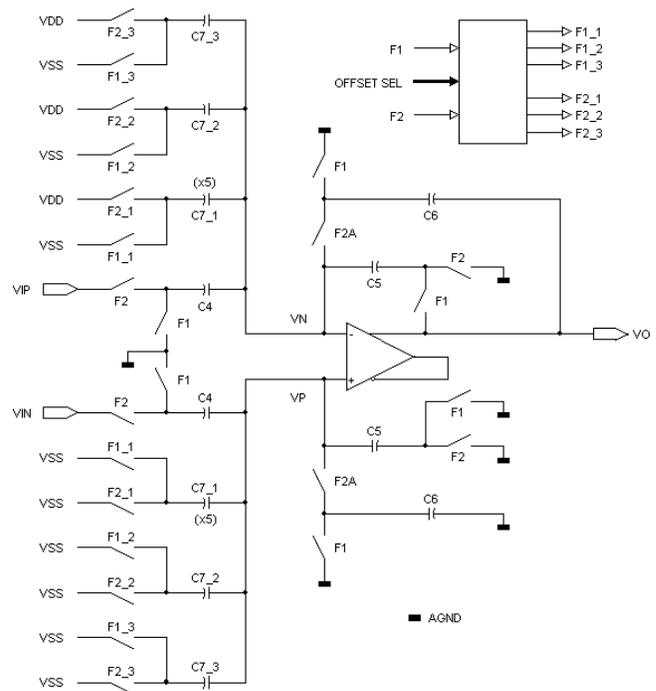


Figure 5. Schematic of the differential to single-ended stage

To allow the op amp to operate in a single-ended configuration, its inverted output was tied to the common-mode feedback terminal to self-bias the NMOS current sources. For unity gain both C_4 and C_5 equal $2C_u$. The offset is introduced through C_7 capacitor array and its respective switches. The offset capacitor size is adjusted to be one tenth of C_u .

Note the offset trimming switches are connected either to V_{DD} or V_{SS} . The offset trimming is attained by properly choosing a specific charge transfer ratio between the offset capacitor array (C_7) and the feedback capacitor (C_5). By default, the offset trimming capacitor is set to $6C_u/10$, so it gives an offset voltage at the output of $0.20 * V_{DD}$. By adding $C_u/10$ to the offset trimming capacitor, the offset voltage will be $0.15 * V_{DD}$ whereas subtracting $C_u/10$ to that the offset voltage becomes $0.25 * V_{DD}$. With such arrangement the output offset voltage of the Differential Amplifier can be trimmed by $\pm 25\%$ around $0.20 * V_{DD}$.

Additionally, it was necessary to design an analog ground generator, a current source for biasing all the circuits, and a clock generator that provides all non-overlapping clock phases necessary to drive the analog switches. As proper circuit operation derives from 2.5V control logic, digital level shifters were included as well.

4. EXPERIMENTAL RESULTS

The Differential Amplifier has been integrated into a SoC realized in a standard 4-metal single-poly 0.25um CMOS process with metal-metal capacitors. Fig. 6 shows a microphotograph of the module with its main sub-blocks outlined. *Clkgen* stands for non-overlapping multi-phase clock generator and *Iref* for current source. The module occupies a silicon area of 0.115 mm^2 ($480\mu\text{m} \times 240\mu\text{m}$) mostly due to large high-linearity capacitor arrays for achieving high accuracy on capacitor ratios.

Silicon evaluation proved the module to be perfectly functional with very good overall performance such as: high linearity, high repeatability, low temperature sensitivity, high power supply rejection ratio and high input common-mode rejection ratio.

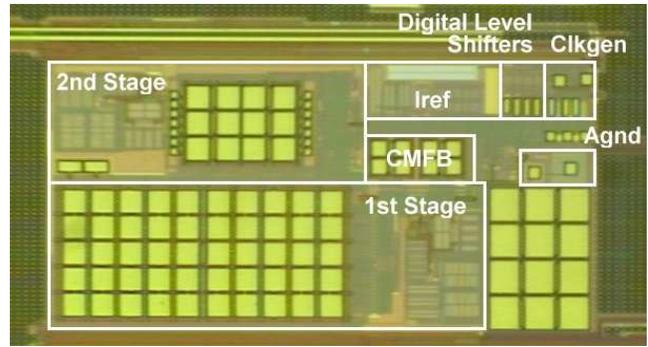


Figure 6. Differential Amplifier microphotograph

As the DA was designed to have its single-ended output sampled by an ADC, there is no access to its internal nodes during normal operation. In a SoC special operating mode, however, some critical nodes are routed to external pins so they can be monitored through the oscilloscope. This feature is achieved at the cost of higher noise injected by the chip into the module. Also the extra routing, bonding and probing in this operating mode add large capacitive loads into its switched-capacitor architecture demanding a slower switching clock and slightly degrading its performance due to leaky phase-to-phase charge transfer.

Fig. 7 illustrates the DA measuring cycle in the SoC special operating mode for zero differential input voltage at 3V power supply. Horizontal and vertical scales are 400us and 0.5V respectively (except ADC trigger signal which is 2V vertical). 1st stage outputs remain at 1.5V while 2nd stage sustains a DC level as determined by the offset selection circuitry. At 80mV differential input, 1st and 2nd stages operate according to Fig. 8.

It is apparent that a fast clocking rate is applied at the beginning. Although this short phase time does not allow for a proper settling time, all DA capacitors are rapidly charged. Once all nodes in the switched-capacitor architecture approach their steady state, the clock rate is reduced and subsequent phase cycles follow to precisely define its output. Since the voltages in a switched-capacitor circuit reach steady state at the end of each phase, the clock is halted at the end of phase 2 (after a defined number of cycles) prior to triggering the ADC with a positive transition in

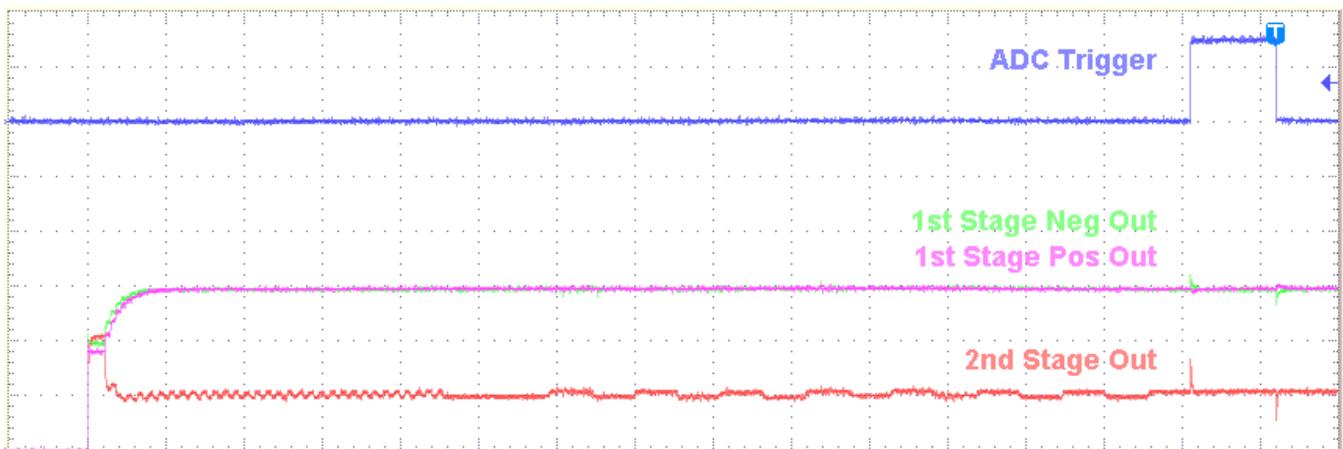


Figure 7. DA waveforms for zero differential input voltage

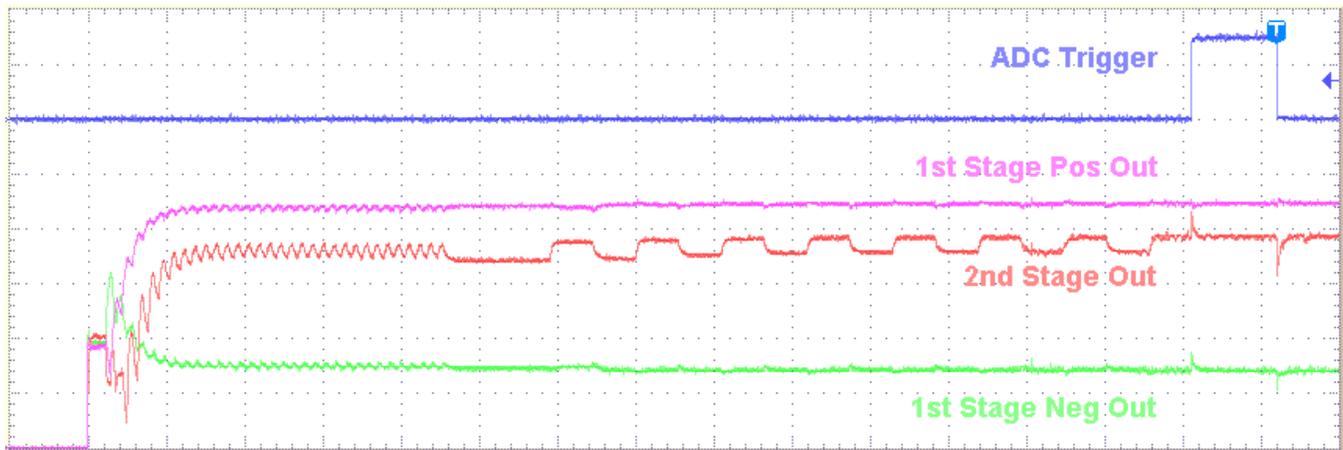


Figure 8. DA waveforms for 80mV differential input voltage

the ADC trigger signal.

5. CONCLUSION

A low-power differential switched-capacitor amplifier for processing a fully-differential input signal coming from a pressure sensor interface has been presented. A SoC device integrating the amplifier has been realized in a 0.25 μ m CMOS technology and silicon results proved the amplifier to be fully operational down to 1.8V with 40 μ A typical supply current. Its very good overall performance derives from its high linearity, high repeatability, high power supply rejection ratio and high common-mode input rejection ratio.

6. REFERENCES

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