EE 140/240A
Spring 2016

Prof. Pister

Homework Assignment #9v2 Solutions

Due by online submission **Monday** 4/11/2015 (Tuesday 9am)

1. Given the choice of NMOS or PMOS input stage, and the four different op-amp topologies that we've talked about (single-stage diff pair with mirror load, two-stage, folded cascode), which combinations are appropriate for the following applications? Assume that the magnitude of the N and P threshold voltages is roughly 0.3V, and that all overdrive voltages are roughly 0.1V.
    a. bandgap reference as in Figure 4.46c driving a 5kΩ load
    b. digital voltage regulator with an output of 1V and a supply of between 1.6 and 3.2V
    c. analog voltage regulator with an output of 1.25V and a supply of between 1.6 and 3.2V
    d. ADC comparator with an input at 1.25V and a supply at 1.25V
    e. variable gain amplifier with an input at 0V and a supply at 1.25V

[5 pts] full credit for some attempt at each

a) driving a 5k load means you need a 2 stage amplifier, otherwise the low load resistance will kill your gain. NMOS is best choice. PMOS might just work, but the input common mode needed is pretty close to the edge with VDD=1.6V

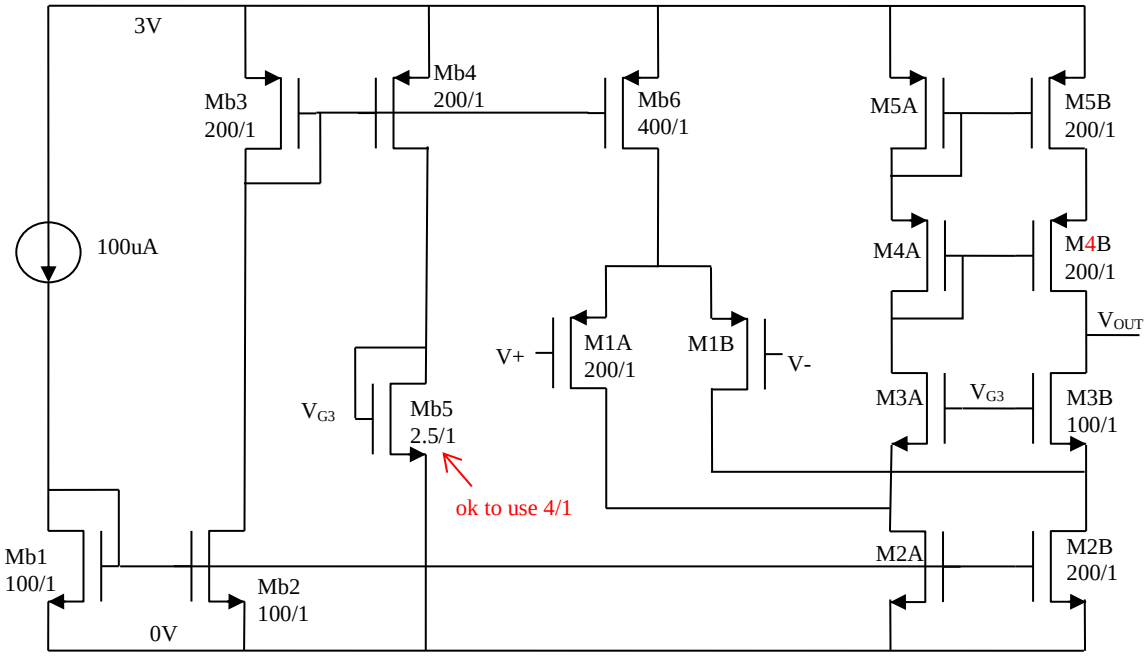
b) NMOS input is the easier choice for common mode swing reasons, but PMOS should work as well. Single stage or two stage is probably best if using an NMOS device to supply the load, due to output swing considerations. Any topology is fine with a PMOS supplying the load (LDO), although it's easiest to use a single stage and not much gain is required.

c) Must use an NMOS here – PMOS common mode input won't work at 1.6V.

d) Must use an NMOS input folded cascode, as that's the only one where the input common mode includes the top rail.

e) Must use a PMOS input folded cascode (and a second stage as we saw later)

2. For the PMOS-input folded cascode op-amp below, assume the following process specs $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ=1/(20V), $-V_{tp}=V_{tn}$=0.3V, C_{ox}=5fF/um^2, C'$_{ol}$=0.5fF/um.



    a. Calculate and tabulate:
        i. the overdrive voltage and current in all devices. For this step you may assume that λ=0. The simplest order may be Mb1 through Mb6, then M1 through M5.
        ii. Calculate the bias voltages on all nodes, assuming $V_{I,CM}$=1V. Specifically: tail, G2, G3, G5, G6, S3B, S4AB, and out.
        iii. the g_m and r_o parameters for M1 through M5

[20 pts] full credit for effort

i) Vov in b1 you can calculate to be 0.1V, and current is clearly 100uA

b2 has the same overdrive as b1 and is the same size, so it also has 100uA. In reality, the drain is likely biased differently (Vdd-|Vtp+Vovp| vs. Vtn+Vovn), so the current will be different, but I said that you could ignore channel length modulation, λ=0).

b3 also has 100uA because of b2. With ½ the mobility but twice the width, it will have the same overdrive, 0.1V

b4 and b6 have the same overdrive as b3, 0.1V. b4 has the same current, 100uA, while b6 was 200uA because it's twice as wide.

b5 has the same current as b4, 100uA. It is 40 times narrower (or 25 if you made the change) than b1, so it will have sqrt(40) or (or sqrt(25) if you made the change) times the overdrive voltage. It turns out that both of these are horrible choices, and lead to a big overdrive of around 0.6 or 0.5V, much bigger than desired. What I *meant* to do was make W5 = 1/5 of W1. Fail.

1AB split the 200uA from b6. Since they have the same current and same size as b3, they must have the same overdrive voltage

	Vov	Id	gm	ro
b1	0.1V	100uA		
b2	0.1V	100uA		
b3	0.1V	100uA		
b4	0.1V	100uA		
b5	0.5—0.6V	100uA		
b6	0.1V	200uA		
1AB	0.1V	100uA	2m	200k
2AB	0.1V	200uA	4m	100k
3AB	0.5—0.6V	100uA	0.4m	200k
4AB	0.1V	100uA	2m	200k
5AB	0.1V	100uA	2m	200k

ii) tail voltage will be Vtp+Vov1 above Vicm, 1-0.3-0.1=0.6

G3 is generated (poorly) by b5. S3 is set by G3, minus Vtn+Vov3

G5 is set by the gate voltage generated by the current flowing through the mirror, 3-0.4=2.6V

G4 is another Vtp+Vov4 below that. S4 is just G5.

node	bias voltage
tail	0.6V
G2	0.4V
G3	0.8 or 0.9V
G4	2.2V
G5	2.6V
S3AB	0.4 or 0.5V
S4AB	2.6

iii) see table above

b. Calculate Gm, Ro, and Av

[3 pts] full credit for effort

Gm = g_{m1} = 100uS

from lecture W11L1, if $\lambda_n=\lambda_p$ and $I_{tail}=I_{D2}$, then Ro = ¼ (g_m r_o) r_o = ¼ (400) 200k = 20M

Av = 2k

c. Calculate the input common mode range and output swing.

[4 pts] full credit for effort

common mode: because the gate of M3 was set poorly, the source is a little too high. The gates of M1AB can get a full threshold below that, or 0.1 or 0.2V depending on which value for Wb5 you used. On the high end, it's Vtp+2Vovp below the top rail, or 2.5V.

Output swing: independent of input common mode, it's a threshold below G3 to a threshold above G4, so 0.4 or 0.6 to 2.2V.

d. What is the minimum voltage that could be used on the gates of M3AB to still keep M2AB in saturation? If you used that voltage, what is the new input common mode range and output swing?

[4 pts] full credit for effort

Min voltage is Vtn+2Vov=0.5V, which sets V_{S3} (and V_{D1}) to 0.1V. Input common mode range on the low end decreases to -0.2V. Output swing on the low end decreases to 0.2V. High end of both is unchanged.

e. If the load capacitance is 1pF (roughly the same as the input capacitance),
   i. what are the pole and unity gain frequencies?
   ii. What is the phase margin?
   iii. What are the frequencies of the pole/zero doublets from the current mirror?

[5 pts] full credit for effort
wp = 1/(RoCL) = 1/(20M * 1pF) = 50 krad/s
wu = Gm/CL = 0.1mS/1pF = 100Mrad/s (quick check: Av*wp=2000*50k=100Mrad/s=wu. good!)
pole frequency of the NMOS cascode transistors should be gm/Cgs=0.1m/0.3p=300 Mrad/s, so that contributes about -20 degrees of phase at the unity gain frequency.
pole/zero double for the mirror should be at gm/(2Cgs5)=0.1m/(1.3p)=80 Mrad/s, so that puts the doublet right at the unity gain frequency, which means another -20 degrees or so. Phase margin should be about 50 degrees.

3. In Figure 2 of this Analog Devices discussion on voltage regulators
   http://www.analog.com/en/design-center/landing-pages/001/fundamentals-of-ldo-design-and-applications.html
   a. Estimate the low-frequency loop gain T= in terms of the op-amp voltage gain A_0, gm of the pass transistor, and load resistance R_L (not shown in the figure).
   b. Why does the SENSE value connect to the positive input of the op-amp? Is this positive feedback?

[3 pts] full credit for effort
a) The gain is $A_0 g_m(R_L \parallel r_{op} \parallel R_1+R_2)$.
b) The second stage (PMOS driving load) has a negative gain. That makes this negative feedback.

4. For the circuit in figure 6.9 in the book
   a. what ratios of C_2 to C_1 are needed to make a variable gain amplifier with gain equal to any integer between 1 and 8?
   b. for a given open-loop op-amp gain A, which of the closed-loop gains above has the worst gain error? (you may assume that C_P=0)

c. if the desired closed-loop gain accuracy is 0.4% regardless of gain setting, what is the minimum open-loop gain necessary for the op-amp?
d. if the amplifier must settle to within 0.4% of the correct value within 10us, what is the minimum unity gain bandwidth of the op-amp?

[4 pts] full credit for effort

a) ratios from 1:1 to 1:8
b) gain error is 1/(Af). It's worst when f is smallest. The smallest f is when the gain is 8, and f=1/9
c) 1/(Af) < 0.4% when f=1/9 → A > 2250
d) an op-amp in feedback with a unity gain ω_u will have a pole at roughly $f\omega_u$ (it's a good approximation if the phase margin is close to 90 degrees) and a corresponding settling time constant $\tau=1/(f\omega_u)$. We need 6 time constants to get to 0.4%, so $6\tau < 10us$. From above, worst-case f=1/9, so $6(9/\omega_u) < 10us$. $\omega_u > 54/10us = 5.4Mrad/s$.

5. In the TI document on SAR ADCs, http://www.ti.com.cn/cn/lit/an/slyt176/slyt176.pdf
   a. does the comparator compare at ground or the top rail?
   b. Assuming a single-sided supply (V_{DDA}, 0) does the voltage on the inputs to the comparator stay between the supply rails?

[2 pts] a) ground; b) no. If the input is more than Vref/2, then when S4 switches to ground on the first bit test, the voltage on V+ will go below ground. This is the opposite configuration to your ADC in the project.