Homework Assignment #6 solutions
Due by online submission Wednesday 3/9/2016 (Thursday at 9am)

1. Check out the datasheet for the K2-W tube op-amp. This op-amp, released in 1952, was the first
    production op-amp. It runs from a +/-300V supply, and has a BW of 300kHz (or k-cycles/s, as
    they said back then – the unit Hertz not having been established yet). There's a schematic on
    page 2. Pins 1, 2, and 6 on the bottom of the figure are V+, V-, and Vout. VR1 and VR2 are
    neon bulbs that provide a low impedance level shift of roughly 100V to center the output
    between the rails. Identify (circle and label):
    a. input differential pair
    b. diff-pair load resistor
    c. tail current resistor. Estimate the common mode gain of the first stage and write it near
        the tail resistor.
    d. Common-cathode gain stage (like CS or CE)
    e. Cathode-follower output stage (like source-follower or emitter follower, CD, CC)
    f. Miller-multiplied compensation capacitor from the output back to the input of the gain
        stage.
    g. Bonus points if you can identify positive feedback in this amplifier, designed to increase
        the low-frequency gain (which ended up at about 20,000).
    [7 pts, 1 for each for parts abdef, 2 pts for c. +1 bonus for g] See scanned solutions.

2. Estimate the output resistance of a CMOS differential amplifier with current mirror load. You
    may assume that $g_m r_o \gg 1$ for all combinations of g_m and r_o. The following steps may help.
    a. Estimate the impedance seen looking into the source of M1A
    b. Estimate the impedance seen looking down from the source of M1B
    c. Estimate the impedance seen looking into the drain of M1B
    d. For the Ro calculation, estimate i_{d1B} as a function of vo.
    e. The current in i_{d2B} is due to both the output resistance and the mirrored current. Estimate
        both parts.
    f. Estimate the total output current io = $i_{d1B} + i_{d2B}$
    g. Show that R_o. is equal to ($r_{o1B} \| r_{o2B}$). Magic!
    [14 pts. 2 each, 1 for effort. Propagating errors only count against you once] See scanned
    solutions.
3. Design a 2-stage NMOS input CMOS op-amp with the following specs:
    a. 20uA tail current
    b. able to sink 100uA from the load
    c. output swing to within 100mV of the rails
    d. input common mode range to within 100mV of the top rail
    Process specs $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=100\mu A/V^2$, $\lambda=1/(5V)$, $-V_{tp}=V_{tn}=0.5V$, $V_{DD}=2V$, $L_{min}=0.5um$,
    $C_{ox}=5fF/um^2$, $C'_{ol}=0.5fF/um$. You may use 1 resistor in your design.
    Draw the schematic, label the device size of each transistor and the bias current flowing in each leg.
    [20 pts. 1 for each W and L of the 8 transistors, 1 for labeling each of the four leg currents.] See
    scanned solutions. There aren't many things that you get to pick in this problem. You can pick
    L_5, and then L_3 and L_6 should be the same. You can pick L_{2A}, and then L_{2B} and L_4 should be the
    same. You can pick L_{1A}, and then L_{1B} should be the same. (W/L) for M3, M4, and M5 are all
    fixed by the specs. You have some flexibility in the overdrive voltage for M1, but V_{ov2} must be
    the same as V_{ov4} (which is set by spec) to get the right bias. Some things to remember:
    $(W/L)_{1a}+(W/L)_{1b}=(W/L)_3$ if their overdrives are the same
    $(W/L)_4 = (W/L)_5$ $(\mu_n C_{ox})/(\mu_p C_{ox})$ if their overdrives are the same
    $(W/L)_{2a}+(W/L)_{2b}=(W/L)_4$ (I_{D3}/I_{D5})

If you pick minimum length (0.5um), minimum overdrive (100mV) for M1, and I_{D6}=10uA, then you get the following table (with additional info for 4b)

	M1ab	M2ab	M3	M4	M5	M6
W/L	10	20	20	200	100	10
W	5u	10u	10u	100u	50u	5u
I_D	10uA	10uA	20uA	100uA	100uA	10uA
V_{ov}	100mV	100mV	100mV	100mV	100mV	100mV
g_m	200uS	200uS	400uS	2mS	2mS	200uS
r_o	500kΩ	500kΩ	250kΩ	50kΩ	50kΩ	500kΩ
C_{gs}	12.5fF	25fF	25fF	250fF	125fF	12.5fF
C_{gd}	2.5fF	5fF	5fF	50fF	25fF	2.5fF

4. For the amplifier in the previous problem,
    [total for the whole problem is 43 pts] See scanned solutions for detail.
    a. carefully draw the allowed input common mode range and output swing
    [8pts. 2 for each line]
    b. calculate and tabulate Id, V_{ov}, g_m, r_o, C_{gs}, and C_{gd} for all devices
    [18pts – ½ pt for each entry in the table above]
    c. calculate the 1st and 2nd stage gain, and the overall gain for both differential and common mode signals.
    [5 pts. 2 each for 1st and 2nd, 1 for overall] -50, -50, 2500
    d. calculate the common mode input range, and the variation in tail current over that range.
    [2 pts] 24%
    e. calculate the gain across Cgd1a.
    [2 pts] I did not mean for this to be a tough problem, but it is if you want to do it right. The simplest answer is $-g_{m1a}/g_{m2a}$=-1. A better answer would take into account the common-mode effect on Vtail, and come up with -1/2. The best answer would use the result from problem 5, and come up with -1/4. Any of those answers is fine. Bottom line: there's not much gain across that node, so not much Millerized input capacitance.
    f. calculate the output pole frequency with a 100fF load capacitance.
    [2 pts] $\omega_{p2} = 1/(R_o\,C_L) = 1/(25k\ 0.1p) = 400$ Mrad/s
    g. calculate the input capacitance of the second stage below the output pole frequency
    [2 pts] Below the output pole C_{gd4} is Millerized, so C_{in2}=250fF+2550fF=2.8pF.
    h. calculate the first stage output pole frequency
    [2 pts] 1.4 Mrad/s
    i. calculate the input capacitance of the second stage above the second stage unity gain frequency
    [2 pts] 0.3pF
5. [240A] Show that the gain from v_{id} to v_{tail} in a diff pair with a current mirror load is +1/4.