EE 140/240A Prof. Pister
Spring 2016

Homework Assignment #4

Due by online submission Wednesday 2/17/2016 (Thursday at 9am)

1. You make measurements on a transistor and find that with the source grounded and the drain voltage at 5V, the drain current increases from 1mA to 4mA as the gate voltage increases from 3V to 4V. When the gate voltage is 4V, the drain current increases from 4mA to 4.1mA when the drain voltage increases from 5V to 6V. What is Vt and lambda for this device? What is gm and ro when the drain voltage is 5V and the gate voltage is 4V? What is the intrinsic gain?
2. You have an PMOS-input common source amplifier with an NMOS load driving a capacitive load. The output is biased at mid-rail. How do ID, gm, ro, Av0, wp, wu, input capacitance, and output swing change if you
    a. triple the width of both devices
    b. triple the width and length of both devices
    c. triple Vov in both devices
3. Using the 0.2um process parameters below, design a common source amplifier with a low-frequency gain of at least 100, and a unity-gain bandwidth of 1.6 GHz while driving a 100fF load. You need an output swing of at least 1V. Make a table of W, L, ID, Vov, gm, ro, for each device, and of Av0, wp, wu, input capacitance, and output swing for the amplifier. You may assume the quadratic model for both FETs, but keep Vov greater than 100mV.
    a. Is the quadratic model likely to be accurate for the bias conditions of your amplifier?
    b. If you wanted to minimize power consumption, how would your design change?
    c. If you wanted to minimize input capacitance, how would your design change?

Process Parameters: C_{ox}=5fF/um^2, C'$_{ol}$=0.5fF/um, $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=100μA/V^2, λ= (0.2um/L)/(10V), -V_{tp}=V_{tn}=0.5V, V_{DD}=2V

4. With $|V_{ds}|$=0.5V, use Cadence to simulate I_d vs V_{gs} from 0 to V_{DD}=1 V for both N and P transistors with W/L= 0.65u/65n and W/L=6.5u/0.65u. (Both are 10/1 aspect ratio, one is short channel, one is long channel).
    a. Plot all of the currents. Do the short channel devices look like our velocity saturation model? Do the long channel devices look quadratic? Perhaps over some range of Vgs?
    b. For the short channel devices, estimate $C_{ox}v_{scl}$ and V_t
    c. Plot sqrt(Id) for the long channel devices (click on the calculator icon to do waveform math). Estimate μC_{ox} and V_t for both N and P devices.
    d. Plot log10(Id) for the short channel devices. Estimate n.
    e. Plot gm for all devices (there's a "deriv" function). What do you expect to see for short channel and long channel devices? In what range of Vgs does the gm of these devices look like it comes from a quadratic or velocity saturated model? Is that consistent with any critical E-field?
    f. Plot gm/Id for all devices. In what device, and at what operating condition, do you get the most bang for the buck (most gm per mA)?
5. For the same devices as above, simulate I_{DS} vs V_{DS} from 0 to V_{DD}=1V with V_{GS}=0.5V.
    a. Plot I_{ds} and r_o on the same plot.
    b. For each device, find the max r_o, and the range of V_{ds} for which $r_o > r_{o,max/2}$
    c. Is $1/(\lambda I_d)$ a good model for output resistance for any/some/all of these devices? (probably no) If no, can you think of any good rule of thumb for design?
6. [ee240A] Using your devices above, generate a 2D surface plot of intrinsic gain vs. Vgs and Vds. What's the maximum gain that you can get?