High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme

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Abstract

A high performance 22/20nm CMOS bulk FinFET achieves the best in-class N/P I_{on} values of 1200/1100 μA/μm for I_{off}=100nA/μm at 1V. Excellent device electrostatic control is demonstrated for gate length (L_{gate}) down to 20nm. Dual-Epitaxy and multiple stressors are essential to boost the device performance. Dual workfunction (WF) with an advanced High-K/Metal gate (HK/MG) stack is deployed in an integration-friendly CMOS process flow. This dual-WF approach provides excellent V_{th} roll-off immunity in the short-channel regime that allows properly positioning the long-channel device V_{th}. Enhanced 193nm immersion lithography has enabled the stringent requirements of the 22/20nm ground rules. Reliability of our advanced HK/MG stack is promising. Excellent SRAM static noise margin at 0.45V is reported.

Introduction

As the requirement of channel length scaling enters sub-30nm regime, the improved electrostatic control of multi-gate device architectures make them attractive for continued transistor channel length scaling in advanced technology nodes. Among the multi-gate architectures, FinFET is the most promising one for its self-aligned multi-gate structure and its relatively better compatibility to the conventional planar CMOS process [1]. However, integrating FinFETs into CMOS process flow in the tight pitch technologies with constrained design rules is demanding. Managing parasitic resistance while maintaining performance is critical for FinFET [2-6]. Proper insertion of multiple stressors on a varying topography is extremely challenging to deploy on the 22/20nm ground rules and beyond.

The influence of long-channel device V_{th} setting on the short-channel device V_{th} roll-off characteristics is well known in device physics particularly when a definite short-channel device V_{th} is required. For a desired short-channel device V_{th} target, a lower long-channel device V_{th} achieves a smaller V_{th} roll-off slope in the short-channel regime and in turn improves process window by suppressing the device performance variation resulting from L_{gate} variation. By using a single-WF metal gate approach, it is difficult to achieve low long-channel device V_{th} for both NFET and PFET simultaneously. Therefore, the capability of separately modulating the metal gate WF of NFET and PFET by the dual-WF approach is critical in achieving variation-tolerant V_{th} roll-off characteristics. However, this important subject has rarely been discussed for FinFET with L_{gate} down to 20nm. In this work, we introduce a dual-WF HK/MG stack in an integrated CMOS process and have compared it with the single-WF approach. Furthermore, we have evaluated and compared the BTI reliability of this advanced dual-WF HK/MG stack to a planar 32nm HK/MG technology [7]

The major objectives of this work are (1) to demonstrate the highly competitive CMOS integrated process for FinFETs on the 22/20nm ground rules, and (2) to provide competitive and comparable NFET/PFET driving currents by carefully deploying process modules and the techniques for effective strain engineering, parasitic source/drain series-resistance (R_{sd}) reduction, and the dual-WF approach. In this paper, we show comparable NFET/PFET strengths (n/p ratio ~1) that allows flexibility in FinFET circuit design architecture and competitive circuit layout with equal device widths.

Process

This paper reports a high performance bulk FinFET architecture using 22/20nm ground rules on wafers with (100) substrate. Advanced 193nm immersion lithography and optimized etching processes were utilized for fin formation, gate patterning and trench contact formation in the front-end integration. The TEM cross-section in Fig. 1 indicates a vertical fin sidewall in the area of device interest and the definition of effective device width (W_{eff} = 2 x Fin Height + Fin Width) in this work. A vertical gate profile from fin-top to fin-bottom at 90nm gate-pitch was achieved (Fig. 2). Good patterning capability is shown in Fig. 3 for a high performance 0.1μm^2 SRAM bit cell.

Proper insertion of stressor films and reduction of parasitic R_{sd} are critical for high performance FinFET. Epitaxial silicon and in-situ boron-doped epitaxial silicon-germanium (e-SiGe) were utilized to enlarge the

current conduction cross-section outside the channel region for NFET and PFET while e-SiGe additionally imposed compressive strain on the PFET channel region for the purpose of improving hole carrier mobility.

Conventional Stress-Memorization-Technique (SMT) [8] was implemented on NFET for electron mobility enhancement. Combining SMT with an optimized N^+ S/D ion-implantation, NFET I_{on} was enhanced by 8% at a constant I_{off} as depicted in Fig. 4. Both mobility enhancement (reduced slope) and R_{sd} reduction (reduced intercept value on the R_total axis) are shown by analyzing R_total vs. L_{gate} curves in Fig. 5. After the conventional nickel-silicide formation, an optimized contact-etch-stop-layer (CESL) was used to provide ~10% improvement in PFET I_{on}-I_{off} performance as shown in Fig. 6.

Our advanced HK/MG process properly adjusted the PFET's WF in order to achieve a low long-channel device V_{th} and excellent V_{th} roll-off slope in the short channel regime that will be discussed more in the next section. More than 25% PFET I_{on}-I_{off} improvement is achieved by combined implementation of the optimized CESL and the gate-last HK/MG stack [9]-[10] as shown in Fig.7. Fig. 8 shows the TEM cross-section of the final gate stack.

Device

Long-channel device V_{th} setting is critical to the V_{th} roll-off characteristics in the short-channel regime. Fig. 9 explains that a higher long-channel device V_{th} (using PFET in the single-WF gate stack as an example) leads to steeper V_{th} roll-off in the short-channel regime and in turn degrades the process window when the goal is to achieve a low short-channel device V_{th}. Our dual-WF approach has successfully lowered the V_{th} of the long-channel devices to <0.3V for both NFET and PFET (Fig. 10). This feature enables improved variation-tolerant V_{th} roll-off characteristics allowing stable short-channel device operation with L_{gate} down to 20nm for high performance device requirements.

Figs. 11-12 show our I_d-V_g and I_d-V_d characteristics. NFET and PFET DIBL of 100mV/V and 120mV/V are reported for devices with 25nm L_{gate}. Sub-threshold swing measures 80mV/decade. Fig. 13 demonstrates N/PFET I_{on}-I_{off} curves achieving I_{on} values of 1200/1100 μA/μm at 100nA/μm I_{off} for V_{dd}=1V. All currents are normalized to W_{eff} as described earlier in Fig. 1. Key contribution of this work is demonstrating state-of-the-art N/PFET devices that meet or exceed the best reported FinFET devices in the industry under stringent design rules. Fig. 14 compares and shows the fact that this work provides the up-to-date overall best NFET and PFET I_{on}-L_{gate} performance.

In contrast with the planar device sharing the same process platform, FinFET shows excellent capability of suppressing the off-state drain-to-bulk junction leakage current (I_{boff}) at a given sub-threshold leakage current as depicted in Fig. 15. This reduced FinFET gated-diode I_{boff} could be partly attributed to a significantly reduced channel doping concentration that is required to sustain the short-channel device V_{th}. As a result, FinFET is especially suitable for the low-standby-power and low-leakage operation.

Reliability

Fig. 16 (a) & (b) exhibit the FinFET PBTI and NBTI performance of our HK/MG stack compared to a planar 32nm HK/MG technology [7]. Our FinFET structure with top and sidewall planes shows similar PBTI/NBTI performance compared to the 32nm planar technology implying that excellent sidewall interface and HK quality is achieved in our optimized FinFET process. Therefore, our FinFET platform maintains good reliability margin as well as high device performance while reducing the process complexity and cost.

SRAM

FinFET width quantization requires extra efforts for the SRAM design to be optimized for the read and write performance by carefully adjusting V_{th} of SRAM transistors. Butterfly curves of the high performance SRAM cell are shown in Fig. 17 at 0.85V, 0.65V and 0.45V respectively. FinFET's improved V_{th} variation and short-channel electrostatic control allow for low operation voltage. Excellent SRAM static noise margin of 90mV is observed even down to 0.45V V_{dd}.

Conclusions

We have successfully demonstrated a high performance and low-leakage FinFET technology on 22/20 nm ground rules. Good electrostatic control down to 20nm L_{gate} was exhibited. By integrating the advanced dual-WF HK/MG stack in FinFET structure, low long-channel device V_{th} and excellent V_{th} roll-off slope in the short-channel regime are achieved for both NFET and PFET. The advantage of dual-WF scheme over single WF scheme is therefore evident. Strain engineering and parasitic R_{sd} reduction endeavors produced highly competitive and balanced N/PFET I_{on}-I_{off} performance.

Reference

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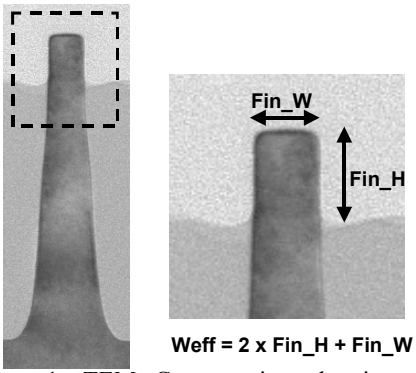

Figure 1. TEM Cross-section showing vertical fin sidewall in the area of interest.

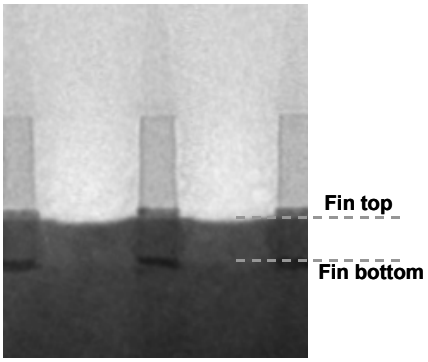

Figure 2. Cross-sectional TEM showing a vertical gate profile from fin-top to fin-bottom.

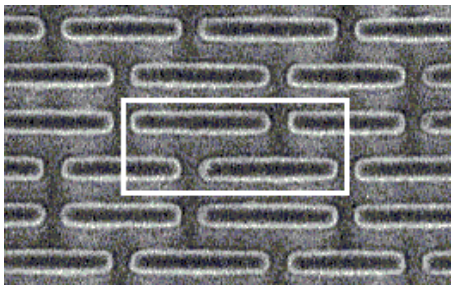

Figure 3. Top view image of the high performance 0.1μm^2 SRAM bit cell showing good pattern fidelity.

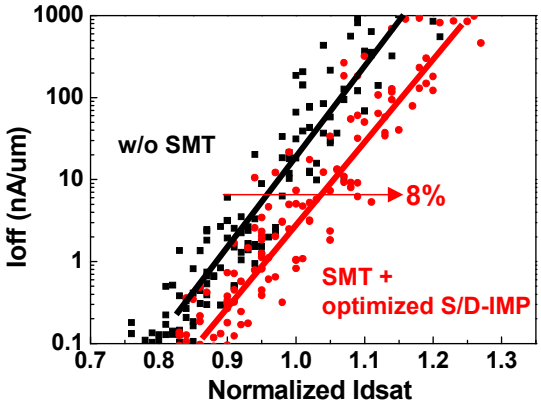

Figure 4. Stress-memorization-technique + optimized N^+ S/D ion-implantation provides 8% I_{on}-I_{off} gain for the NFET.

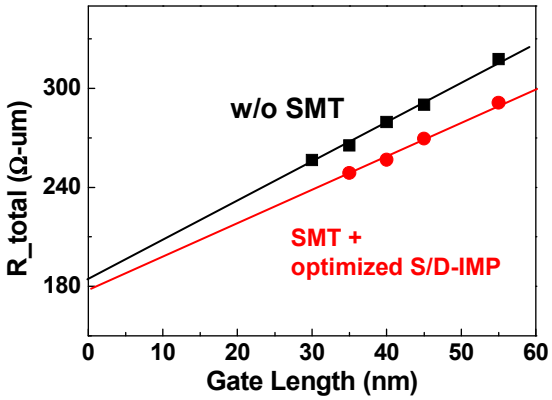

Figure 5. SMT stress + optimized N^+ S/D ion-implantation demonstrates mobility enhancement (lower slope) and R_{sd} reduction (lower intercept) for the NFET.

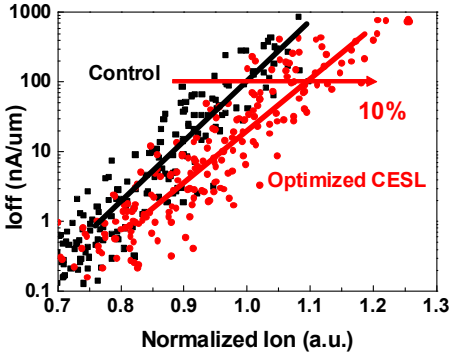

Figure 6. Optimized CESL leads to 10% better PFET I_{on}-I_{off} over the control sample.

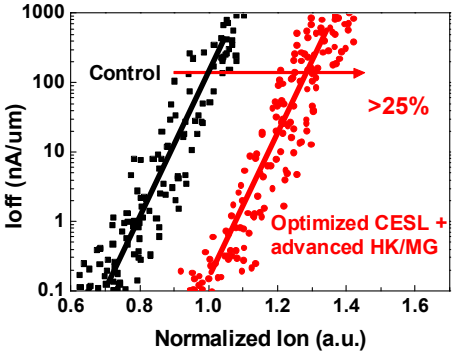

Figure 7. Optimized CESL + Advanced HK/MG improves PFET I_{on}-I_{off} by > 25%. Our Advanced HK/MG provides not only correct WF setting, but also improved strain efficiency.

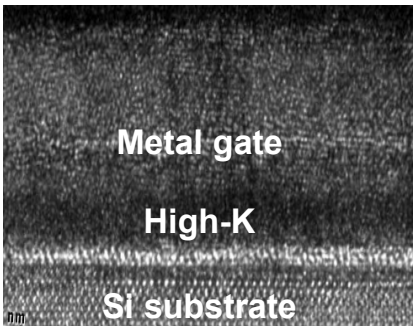

Figure 8. Cross-sectional TEM of the advanced HK/MG scheme.

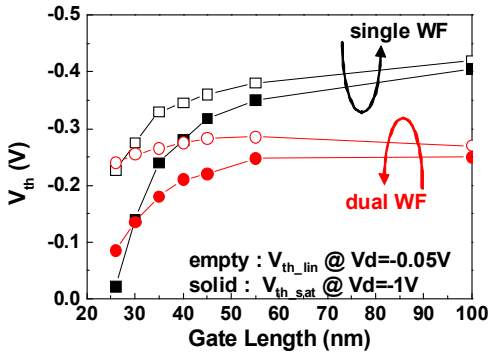

Figure 9. Higher long-channel V_{th} leads to steeper V_{th} roll-off slope in the short-channel regime. By independently optimizing WF for PFET in the dual WF case, improved V_{th} roll-off slope is achieved.

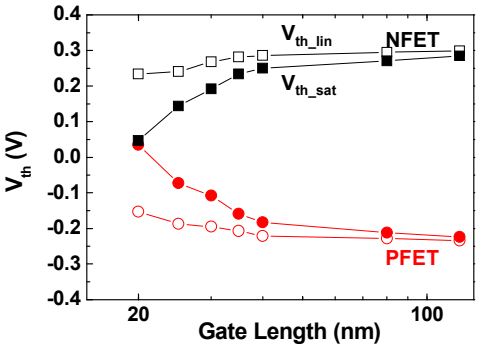

Figure 10. V_{th} vs. L_{gate} characteristics for both NFET and PFET using the advanced HK/MG scheme in this work. Long-channel V_{th} achieves <0.3V.

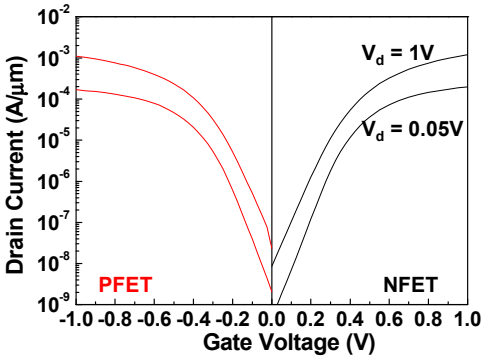

Figure 11. Id-Vg curves for 25nm L_{gate} NFET and PFET.

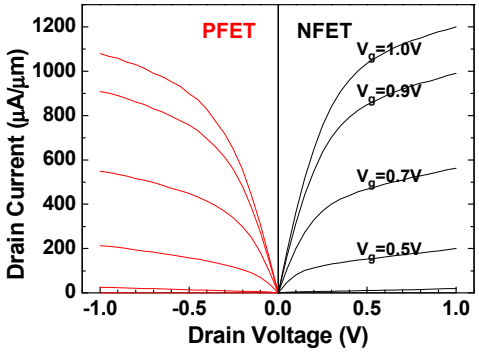

Figure 12. Id-Vd curves for 25nm L_{gate} NFET and PFET

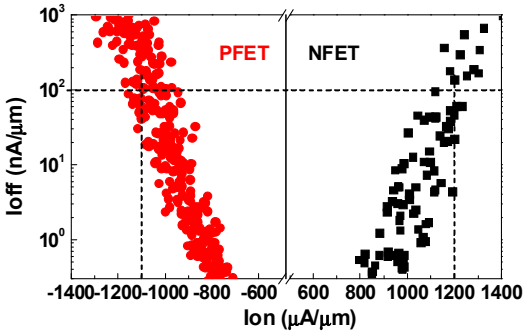

Figure 13. I_{on}-I_{off} curves show I_{on} = 1200 μA/μm for NFET and 1100 μA/μm for PFET at I_{off} = 100nA/μm at V_{dd}=1V.

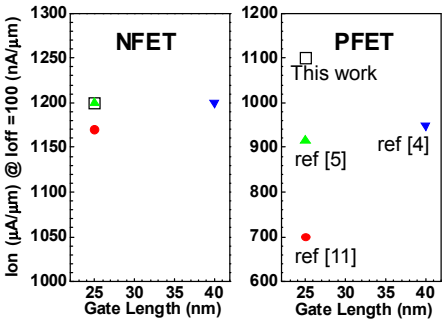

Figure 14. Performance benchmark of I_{on}-L_{gate} at I_{off} = 100nA/μm for the previous FinFET works.

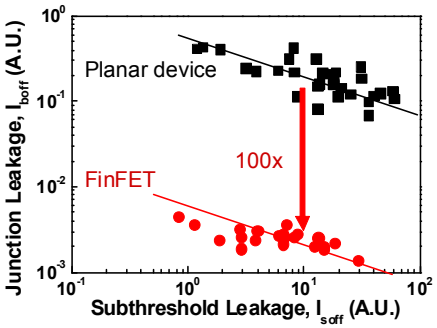

Figure 15. N-FinFETs junction leakage decreases by 100 times at the same I_{soff} leakage compared to the planar NFETs using similar process conditions.

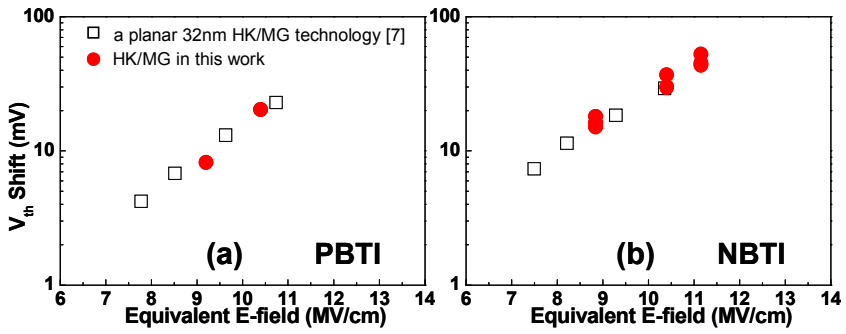

Figure 16. Advanced HK/MG scheme used in this work shows similar PBTI and NBTI performance to a planar 32nm HK/MG technology [7].

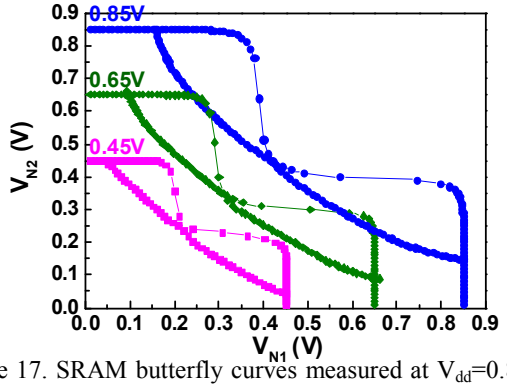

Figure 17. SRAM butterfly curves measured at V_{dd}=0.85V, 0.65V and 0.45V. Excellent static noise margin of 90mV is observed at V_{dd}=0.45V.