Energy Efficiency Enhancement in Mobile Processor Cache Memory Design Using Emerging Nonvolatile Memory

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Motivation
Memory hierarchy design creates an illusion of a high-speed and large-capacity memory by utilizing different types of memories. L1 cache implemented by SRAM reduces the latency between CPU and main memory. However, as technology scaling, increasing leakage power for SRAM has posed challenges to circuit and architecture designs in future memory hierarchy. In the mean time, emerging memory technologies, such as STT-RAM, PCM and RRAM, are being explored as potential alternatives to existing memories in future computing systems. Such nonvolatile memory technology, combining the speed of SRAM, the density of DRAM and the non-volatility of flash memory, offers a tremendous opportunity for low-power solution in mobile processors.

Cross-point RRAM Architecture
RRAM is one of the most promising next-generation nonvolatile memories. To achieve the highest memory density, cross-point RRAM is proposed instead of conventional 1T1R scenario [1]. Furthermore, since the memory elements are fabricated between metal layers, even higher array efficiency can be achieved by hiding peripheral circuits underneath the multi-layer cross-point memory array [2-3]. However, in absence of the selector, a large amount of leakage current flowing through unselected cell is inevitable [4]. In order to alleviate the leakage current issues and reduce disturb problems, several circuit techniques and optimal block size should be employed.

Energy Analysis
We propose a cross-point RRAM circuit with energy analysis of different cell resistance values, write current and block sizes. Also, a SRAM with same capacity will be used to compare with the proposed RRAM in area, energy and speed aspect. Finally, we will evaluate the pros and cons of utilizing RRAM as cache to increase energy efficiency in mobile applications. RRAM peripheral circuit will be built with device characterization ability [5] to measure chip features.

References