IRAM: A Microprocessor for the Post-PC Era

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Perspective on Post-PC Era

PostPC Era will be driven by 2 technologies:

1) Mobile Consumer Devices
   – e.g., successor to PDA, cell phone, wearable computers

2) Infrastructure to Support such Devices
   – e.g., successor to Big Fat Web Servers, Database Servers
A Better Media for Mobile Multimedia MPUs: Logic+DRAM

- Crash of DRAM market inspires new use of wafers
- Faster logic in DRAM process
  - DRAM vendors offer faster transistors + same number metal layers as good logic process? @ ≈ 20% higher cost per wafer?
- Called Intelligent RAM (“IRAM”) since most of transistors will be DRAM
IRAM Vision Statement

Microprocessor & DRAM on a single chip:

- on-chip memory latency 5-10X, bandwidth 50-100X
- improve energy efficiency 2X-4X (no off-chip bus)
- serial I/O 5-10X v. buses
- smaller board area/volume
- adjustable memory size/width
Potential Multimedia Architecture

“New” model: VSIW=Very Short Instruction Word!
- Compact: Describe N operations with 1 short instruct.
- Predictable (real-time) performance vs. statistical performance (cache)
- Multimedia ready: choose N*64b, 2N*32b, 4N*16b
- Easy to get high performance
- Compiler technology already developed, for sale!
  » Don’t have to write all programs in assembly language
Revive Vector (= VSIW) Architecture!

- Cost: $1M each?
- Low latency, high BW memory system?
- Code density?
- Compilers?
- Performance?
- Power/Energy?
- Limited to scientific applications?

- Single-chip CMOS MPU/IRAM
- IRAM
- Much smaller than VLIW
- For sale, mature (>20 years)
- Easy scale speed with technology
- Parallel to save energy, keep perf
- Multimedia apps vectorizable too: N*64b, 2N*32b, 4N*16b
V-IRAM 1: 0.18 µm, Fast Logic, 200 MHz
1.6 GFLOPS(64b)/ 6.4 GOPS(16b)/ 16MB

2-way Superscalar Processor

16K I cache
16K D cache

Instruction Queue

Load/Store

Vector Registers

Memory Crossbar Switch

I/O

Serial I/O

4 x 64 or
8 x 32 or
16 x 16
Tentative VIRAM-1 Floorplan

- Ring-based Switch
- Memory (128 Mbits / 16 MBytes)
- 4 Vector Pipes/Lanes
- CPU +$
- Memory (128 Mbits / 16 MBytes)

- 0.18 µm DRAM
  16-32 MB in 16 banks x 256b
- 0.18 µm, 5 Metal Logic
- ≈ 200 MHz MIPS IV, 16K I$, 16K D$
- ≈ 4 200 MHz FP/int. vector units
- die: ≈ 20x20 mm
- xtors: ≈ 130-250M
- power: ≈ 2 Watts
## VIRAM-1 Simulated Performance

<table>
<thead>
<tr>
<th>Kernel</th>
<th>GOPS</th>
<th>% Peak</th>
<th>Cycles/pixel (small=fast)</th>
<th>VIRAM</th>
<th>MMX TMS‘C82</th>
</tr>
</thead>
<tbody>
<tr>
<td>16b Compositing</td>
<td>6.40</td>
<td>100%</td>
<td>0.13</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>16b iDCT</td>
<td>3.10</td>
<td>48%</td>
<td>0.75</td>
<td>3.75</td>
<td>5.70</td>
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<tr>
<td>32b Color</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion</td>
<td>2.95</td>
<td>92%</td>
<td>0.78</td>
<td>8.00</td>
<td>--</td>
</tr>
<tr>
<td>32b</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Convolution</td>
<td>3.16</td>
<td>99%</td>
<td>1.21</td>
<td>5.49</td>
<td>6.50</td>
</tr>
<tr>
<td>32b FP Matrix</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multiply</td>
<td>3.19</td>
<td>97%</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>
Tentative VIRAM -”0.25” Floorplan

- Demonstrate scalability via 2nd layout (automatic from 1st)
- 8 MB in 2 banks x 256b, 32 subbanks
- ≈ 200 MHz CPU, 8K I$, 8K D$
- 1 ≈ 200 MHz FP/int. vector units
- die: ≈ 5 x 20 mm
- xtors: ≈ 70M
- power: ≈ 0.5 Watts

<table>
<thead>
<tr>
<th>Kernel</th>
<th>GOPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comp.</td>
<td>6.40</td>
</tr>
<tr>
<td>iDCT</td>
<td>3.10</td>
</tr>
<tr>
<td>CLR.Conv.</td>
<td>2.95</td>
</tr>
<tr>
<td>Conv.</td>
<td>3.16</td>
</tr>
<tr>
<td>FP Matrix</td>
<td>3.19</td>
</tr>
</tbody>
</table>
V-IRAM-1 Tentative Plan

- Phase I: Feasibility stage (≈H2’98)
  - Test chip, CAD agreement, architecture defined
- Phase 2: Design & Layout Stage (≈’99)
  - Test chip, Simulated design and layout
- Phase 3: Verification (≈1Q’00)
  - Tape-out Q2’00
- Phase 4: Fabrication, Testing, and Demonstration (≈3Q’00)
  - Functional integrated circuit

- 100M transistor microprocessor before Intel?
IRAM not a new idea

Stone, '70 “Logic-in memory”
Barron, '78 “Transputer”
Dally, '90 “J-machine”
Patterson, ‘90 panel session
Kogge, ‘94 “Execube”

- SIMD on chip (DRAM)
- Uniprocessor (SRAM)
- MIMD on chip (DRAM)
- Uniprocessor (DRAM)
- MIMD component (SRAM)

Computational RAM
IRAM Chip Challenges

- Merged Logic-DRAM process: Cost of wafer, Impact on yield, testing cost of logic and DRAM
- Price of on-chip DRAM vs. separate DRAM chips?
- Time delay of transistor speeds, memory cell sizes in Merged process vs. Logic only or DRAM only
- DRAM block: flexibility via DRAM “compiler” (very size, width, no. subbanks) vs. fixed block;
  - synchronous interface available?
- Applications: advantages in memory bandwidth, energy, system size to offset above challenges?
- Emotion Engine: 6.2 GFLOPS, 75 million polygons per second (Microprocessor Report, 13:5)
  - Superscalar MIPS core + vector coprocessor + graphics/DRAM
  - Claim: *Toy Story* realism brought to games!
Infrastructure for Next Generation

- Servers today based on desktop MPUs: Central Processor Units + Peripheral Disks
- What would servers look like if based on mobile, multimedia microprocessors?
- Include processor, network interface inside disk
- ISTORE: a HW/software architecture for building scaleable, self-maintaining storage
  - An introspective system: processor/disk ⇒ it monitors itself and acts on its observations
  - No administrators to configure, monitor, tune
ISTORE-I Hardware

- ISTORE uses “intelligent” hardware

Intelligent Chassis: scaleable, redundant, fast network + UPS

CPU, memory, NI

Device

Intelligent Disk “Brick”: a disk, plus a fast embedded CPU, memory, and redundant network interfaces
IRAM Conclusion

- IRAM potential in mem/IO BW, energy, board area; challenges in power/performance, testing, yield
- 10X-100X improvements based on technology shipping for 20 years (not JJ, photons, MEMS, ...)
- Suppose IRAM is successful
- Revolution in computer implementation
  - Potential Impact #1: turn server industry inside-out?
- Potential #2: shift semiconductor balance of power?
  Who ships the most memory? Most microprocessors?
Acknowledgments

■ Looking for ideas of VIRAM enabled apps
■ Contact us if you’re interested:
   email: patterson@cs.berkeley.edu
   http://iram.cs.berkeley.edu/
■ Thanks for advice/support: DARPA, California MICRO, Hitachi, IBM, Intel, LG Semicon, Microsoft, Neomagic, Sandcraft, SGI/Cray, Sun Microsystems, TI, TSMC
Backup Slides

(The following slides are used to help answer questions)
Commercial IRAM highway is governed by memory per IRAM?
Near-term IRAM Applications

■ “Intelligent” Set-top
  – 2.6M Nintendo 64 (∼ $150) sold in 1st year
  – 4-chip Nintendo ⇒ 1-chip: 3D graphics, sound, fun!

■ “Intelligent” Personal Digital Assistant
  – 0.6M PalmPilots (∼ $300) sold in 1st 6 months
  – Handwriting + learn new alphabet (α = K, ⊣ = T, ⊼ = 4)
    v. Speech input
Words to Remember

“...a strategic inflection point is a time in the life of a business when its fundamentals are about to change. ... Let's not mince words: A strategic inflection point can be deadly when unattended to. Companies that begin a decline as a result of its changes rarely recover their previous greatness.”

– Only the Paranoid Survive, Andrew S. Grove, 1996
IBM MicroDrive
- 1.7” x 1.4” x 0.2”
- 1999: 340 MB, 5400 RPM, 5 MB/s, 15 ms seek
- 2006: 9 GB, 50 MB/s?

ISTORE node
- MicroDrive + IRAM

Crossbar switches growing by Moore’s Law
- 16 x 16 in 1999 ⇒ 64 x 64 in 2005

ISTORE rack (19” x 33” x 84”)
- 1 tray (3” high) ⇒ 16 x 32 ⇒ 512 ISTORE nodes
- 20 trays+switches+UPS ⇒ 10,240 ISTORE nodes(!)