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Solution #3

Solutions 3
CS252 Graduate Computer Architecture

6.6

IOs per second = $\frac{1}{\text{accesstime}}$

access time = seek time + rotational delay + transfer time + controller overhead
controller overhead = 1ms
rotational delay = $\frac{\text{10033rotations}}{\text{60seconds}}$ = 167 rot/sec = 5.98 ms/rot = 2.99 ms delay
a = $\frac{-10(.98)+15(7.71)-5(18.2)}{3\sqrt{6526}}$ = .061275
b = $\frac{7(.98)-15(7.71)+8(18.2)}{3\times 6526}$ = .0018802
c = .98
average distance = 1500 tracks
seek time = $.061275 \times \sqrt{\text{Distance} - 1} + .0018802 \times (\text{Distance} - 1) + .98 = 6.17$ ms

The transfer time depends on which disk organization we have.

single disk transfer time = $\frac{\text{60seconds}}{\text{10033rotations}} \times (\frac{8}{171} rotations)$ = .280ms
array transfer time = 1/4 of single disk time = .070 ms

The access time for the single disk is then 6.17 + 2.99 + .280 + 1.00 ms, or 10.44 ms. This equals 96 IOPS, or 383 KB/s.

The access time for the array is 6.17 + 2.99 + .07 + 1.00 ms, 10.23 ms. This equals 98 IOPS, or 391 KB/s.

6.10

	% of total	cycles	reads	writes
load	22.8	2	2	0
store	14.3	2	1	1
other	62.9	1	1	0

mem access / instr = 1 + .143 + .228 = 1.371
reads / instr = 1 + .228 = 1.228
writes / instr = .143 = .143
perfect CPI = 1(.629) + 2(.228) + 2(.143) = 1.371
% of mem refs that are reads = 1.228/1.371 = 90%

For the write-through:

type	% of all refs	stall cycles
read hit	(% reads $\times$ % hits) = .9 $\times$ .95 = 85.5	0
write hit	(% writes $\times$ % hits) = .1 $\times$ .95 = 9.5	16
read miss	(% reads $\times$ % miss) = .9 $\times$ .05 = 4.5	23
write miss	(% writes $\times$ % miss) = .1 $\times$ .05 = .5	39

stall cycles per access = .095(16) + .045(23) + .005(39) = 2.75

For the write-back:

type	% of all refs	stall cycles
hit	% hits = .95	0
miss, block clean	(% miss $\times$ % clean) = .05 $\times$ .7 = 3.5	23
miss, block dirty	(% miss $\times$ % dirty) = .05 $\times$ .3 = 1.5	31

stall cycles per access = .035(23) + .015(31) = 1.27

a) Traffic ration is the ratio of the stall cycles to the total cycles.
$TR_{\text{writethrough}} = \frac{2.75}{1+2.75} = 73.3\%$
$TR_{\text{writeback}} = \frac{1.27}{1+1.27} = 56.0\%$

b) The remaining available bandwidth is:
write through: 80% - 73.3% = 6.7%
write back: 80% - 56.0% = 24.0%

c) First, we figure out how many cycles it takes to execute 1 million instructions:
$T_{\text{writethrough}} = (1.371 + (3.75 \times 1.371))$ CPI $\times$ 1 million instructions = 6.51 million cycles
$T_{\text{writeback}} = (1.371 + (2.27 \times 1.371))$ CPI $\times$ $\times$ 1 million instructions = 4.48 million cycles

We need to use the bus at the beginning of the access (the initiation) and at the end of the access (the transfer). During this time, we need access to the bus for 1000 cycles. We only have some of the bus bandwidth available to us, so the bus accesses will take longer than 1000 cycles. The total time for the accesses are:
$T_{\text{writethrough}} = 1000/.067 + 100000 + 1000/.067 = 130\text{k cycles}$
$T_{\text{writeback}} = 1000/.24 + 100000 + 1000/.24 = 108\text{k cycles}$

The number of disks reads possible is then:
write through: $\frac{6.51\times10^6}{130\times10^3} = 50.1$ transfers
write back: $\frac{4.48\times10^6}{108\times10^3} = 41.5$ transfers

If the cache miss rate is cut in half, the write through stalls per access is (.1*.975*16) + (.9*.025*23) + (.1*.025*39) = 2.175; the write back stalls per access is (.025*.7*23) + (.025*.3*31) = .635. The traffic ratio for the write through is 2.175/3.175 = 68.5%; the traffic ratio for the write back is

.635/1.635 = 38.8%. The available bandwidth for the write through is 11.5%; for the write back, 41.2%. The total time for the write through access is now 118k cycles; for the write back, 105k cycles. The number of reads possible for the write through is (1.371 + 2.175*1.371/.118) = 36.9; for the write back, (1.371 + .635*1.371/.105) = 21.3.

d) For this problem, we can either be initiating or transferring constantly. In steady state, we can effectively complete a write through access in 2000/.067 = 30k instructions, and a write back access in 2000/.24 = 8k instructions. This means that the write through can complete 3750/30 = 125 accesses, and the write back can complete 2270/8 = 284 accesses.

7.3 T1 transfer time $= 10^{11}$ bytes $\times \frac{\text{sec}}{.75\times 10^{6}\text{bits}} \times$ 8bitsbyte = 1066667 seconds = 12 days
Ethernet transfer time $= 10^{11}$ bytes $\times \frac{\text{sec}}{5\times 10^{6}\text{bits}} \times$ 8bitsbytes = 160000 seconds = 44 hours
Overnight time = 15 hours

No, neither network will get the data there first. The overnight bandwidth is $\frac{8\times 10^{11}\text{bytes}}{54000\text{seconds}} = 14.8$ Mb/s, or 1.85 MB/s.

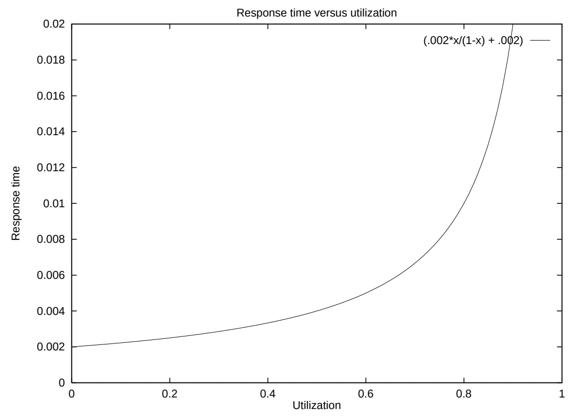
7.13

a) u = arrival rate / service rate = 200/(1/.002) = .4

b) $T_Q = T_S \times \frac{u}{1-u}$ = (.002)(.6667) = 1.33 ms
Number in gateway = arrival rate $\times$ ($T_Q + T_S$) = 200 $\times$ (.002 + .00133) = .67

c) Mean time = 3.33 ms

d)



e) We would have overflow is we would have 12 messages in the system.
$.4^{12}$ = .00168%.

f) $.4^n = .000001$
$\log_{.4}(.4^n) = n = \log_{.4}(.000001) = 15.077$
So, we must be able to handle 15 messages in the system without overflow. This means that we need a FIFO length of 14 messages.