University of California, Berkeley
College of Engineering
Computer Science Division — EECS

Spring 1998 D.A. Patterson

Assignment 2
Excercises due Thursday, February 26 in 283 Soda by 5PM.
CS252 Graduate Computer Architecture

For this homework, you should work in pairs. Your partner can not be the person you worked with for HW1. Do excercises B.4, 5.5, and 5.8. In addition, do the following problem.

You are asked to design hardware organization for a video decoding system. Assume the following:

- The video decoding algorithm is composed of two parts: a non-parallelizable part that accounts for 20% of the instructions, and a parallelizable part that accounts for 80% of the instructions.
- The parallelizable part parallelizes perfectly.
- Decoding one frame takes 2M instructions.
- The design constrains you to using 1, 2, 4, or 8 processors.
- The processor consumes the same energy every cycle, whether it is doing useful work or not (there is no suspend mode).

The processor that you can use has the following characteristics:

Supply Voltage (V)	Frequency (Mhz)	Power (mW)
2.7	33	490
2.3	25	290
2.2	20	190
2.0	16	130

a) What is the organization that gives the highest performance? How many frames/sec does it deliver? What is the power consumed? What is the energy consumed per frame?

b) What is the organization that gives us the best energy efficiency? How many frames/sec does it deliver? What is the power consumed? What is the energy consumed per frame?

c) Suppose that we are designing a portable unit that will have to decode 15 frames/sec. What organization should we use? What is the energy consumed per frame?