Review

- Caches contain all information on state of cached memory blocks
- Snooping and Directory Protocols similar
- Bus makes snooping easier because of broadcast (snooping $\rightarrow$ Uniform Memory Access)
- Directory has extra data structure to keep track of state of all cache blocks
- Distributing directory $\Rightarrow$ scalable shared address multiprocessor
  $\Rightarrow$ Cache coherent, Non Uniform Memory Access (NUMA)

Parallel App: Commercial Workload

- Online transaction processing workload (OLTP) (like TPC-B or -C)
- Decision support system (DSS) (like TPC-D)
- Web index search (Altavista)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>User % Time</th>
<th>Kernel % Time</th>
<th>I/O % Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>OLTP</td>
<td>71%</td>
<td>18%</td>
<td>11%</td>
</tr>
<tr>
<td>DSS (range)</td>
<td>82-94%</td>
<td>3-5%</td>
<td>4-13%</td>
</tr>
<tr>
<td>DSS (avg)</td>
<td>87%</td>
<td>4%</td>
<td>9%</td>
</tr>
<tr>
<td>Altavista</td>
<td>&gt; 98%</td>
<td>&lt; 1%</td>
<td>&lt; 1%</td>
</tr>
</tbody>
</table>

OLTP Performance as vary L3$ size

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Normalized Execution Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MB</td>
<td>100</td>
</tr>
<tr>
<td>2 MB</td>
<td>90.8</td>
</tr>
<tr>
<td>4 MB</td>
<td>81.6</td>
</tr>
<tr>
<td>8 MB</td>
<td>72.4</td>
</tr>
</tbody>
</table>

OL3 Miss Breakdown

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Memory Cycles per Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MB</td>
<td>0.25</td>
</tr>
<tr>
<td>2 MB</td>
<td>0.5</td>
</tr>
<tr>
<td>4 MB</td>
<td>0.75</td>
</tr>
<tr>
<td>8 MB</td>
<td>1.0</td>
</tr>
</tbody>
</table>

Alpha 4100 SMP

- 4 CPUs
- 300 MHz Apha 211264 @ 300 MHz
- L1$ 8KB direct mapped, write through
- L2$ 96KB, 3-way set associative
- L3$ 2MB (off chip), direct mapped
- Memory latency 80 clock cycles
- Cache to cache 125 clock cycles
Memory CPI as increase CPUs

<table>
<thead>
<tr>
<th>Processor count</th>
<th>Instruction</th>
<th>Conflict/Capacity</th>
<th>Cold</th>
<th>False Sharing</th>
<th>True Sharing</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>1.5</td>
<td>1.0</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
<td>2.0</td>
<td>1.0</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>4</td>
<td>0.5</td>
<td>2.5</td>
<td>1.5</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>6</td>
<td>0.5</td>
<td>3.0</td>
<td>2.0</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>8</td>
<td>0.5</td>
<td>3.5</td>
<td>2.5</td>
<td>2.0</td>
<td>2.0</td>
</tr>
</tbody>
</table>

OLTP Performance as vary L3$ size

<table>
<thead>
<tr>
<th>Block size in bytes</th>
<th>Instruction</th>
<th>Capacity/Conflict</th>
<th>Cold</th>
<th>False Sharing</th>
<th>True Sharing</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>64</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>128</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>9</td>
<td>12</td>
</tr>
<tr>
<td>256</td>
<td>0</td>
<td>4</td>
<td>8</td>
<td>12</td>
<td>16</td>
</tr>
</tbody>
</table>

NUMA Memory performance for Scientific Apps on SGI Origin 2000

- Show average cycles per memory reference in 4 categories:
  - Cache Hit
  - Miss to local memory
  - Remote miss to home
  - 3-network hop miss to remote cache

CS 252 Administrivia

- Quiz #1 Wed March 7 5:30-8:30 306 Soda
  - No Lecture
- La Val's afterward quiz: free food and drink
- 3 questions
- Bring pencils
- Bring sheet of paper with notes on 2 sides
- Bring calculator (but don't store notes in calculator)

SGI Origin 2000

- a pure NUMA
- 2 CPUs per node
- Scales up to 2048 processors
- Design for scientific computation vs. commercial processing
- Scalable bandwidth is crucial to Origin

Parallel App: Scientific/Technical

- FFT Kernel: 1D complex number FFT
  - 2 matrix transpose phases => all-to-all communication
  - Sequential time for n data points: O(n log n)
  - Example is 1 million point data set
- LU Kernel: dense matrix factorization
  - Blocking helps cache miss rate, 16x16
  - Sequential time for n matrix: O(n^3)
  - Example is 512 x 512 matrix
Parallel App: Scientific/Technical

- **Barnes App**: Barnes-Hut n-body algorithm solving a problem in galaxy evolution
  - n-body algs rely on forces drop off with distance; if far enough away, can ignore (e.g., gravity is 1/d^2)
  - Sequential time for n data points: O(n log n)
  - Example is 16,384 bodies
- **Ocean App**: Gauss-Seidel multigrid technique to solve a set of elliptical partial differential eq.s
  - red-black Gauss-Seidel colors points in grid to consistently update points based on previous values of adjacent neighbors
  - Multigrid solve finite diff. eq. by iteration using hierarchy Grid
  - Communication when boundary accessed by adjacent subgrid
  - Sequential time for non grid: O(n^2)
  - Input: 130 x 130 grid points, 5 iterations

Cross Cutting Issues: Performance Measurement of Parallel Processors

- **Performance**: how well scale as increase Proc
- **Speedup** fixed as well as scaleup of problem
  - Assume benchmark of size n on p processors makes sense: how scale benchmark to run on m * p processors?
  - **Memory-constrained scaling**: keeping the amount of memory used per processor constant
  - **Time-constrained scaling**: keeping total execution time, assuming perfect speedup, constant
- **Example**: 1 hour on 10 P, time ~ O(n^3), 100 P?
  - Time-constrained scaling: 1 hour, => 10/10 = 2.15m scale up
  - Memory-constrained scaling: 10m size => 10/10 = 10X or 100 hour/100X processors for 100X longer???
  - Need to know application well to scale: # iterations, error tolerance
Cross Cutting Issues: Memory System Issues

- Multilevel cache hierarchy + multilevel inclusion—every level of cache hierarchy is a subset of next level—then can reduce contention between coherence traffic and processor traffic
- Hard if cache blocks different sizes
- Also issues in memory consistency model and speculation, nonblocking caches, prefetching

Example: Sun Wildfire Prototype

- To reduce contention for page, has Coherent Memory Replication (CMR)
- Page-level mechanisms for migrating and replicating pages in memory, coherence is still maintained at the cache-block level
- Page counters record misses to remote pages and to migrate/replicate pages with high count
- Migrate when a page is primarily used by a node
- Replicate when multiple nodes share a page

Example: Sun Wildfire Prototype

- Connect 2-4 SMPs via optional NUMA technology
- Use “off-the-shelf” SMPs as building block
- For example, E6000 up to 15 processor or I/O boards (2 CPUs/board)
- Gigaplane bus interconnect, 3.2 Gbytes/sec
- Wildfire Interface board (WFI) replace a CPU board => up to 112 processors (4 x 28)
- WFI board supports one coherent address space across 4 SMPs
- Each WFI has 3 ports connect to up to 3 additional nodes, each with a dual directional 800 MB/sec connection
- Has a directory cache in WFI interface: local or clean OK, otherwise sent to home node
- Multiple bus transactions

Memory Latency Wildfire v. Origin (nanoseconds)

<table>
<thead>
<tr>
<th>Case</th>
<th>How?</th>
<th>Target?</th>
<th>Wildfire</th>
<th>Origin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local mem.</td>
<td>Restart</td>
<td>Unowned</td>
<td>342</td>
<td>338</td>
</tr>
<tr>
<td>Local mem.</td>
<td>Restart</td>
<td>Dirty</td>
<td>482</td>
<td>892</td>
</tr>
<tr>
<td>Avg. remote</td>
<td>Restart</td>
<td>Unowned</td>
<td>1774</td>
<td>973</td>
</tr>
<tr>
<td>Avg. remote</td>
<td>Restart</td>
<td>Dirty</td>
<td>2162</td>
<td>1531</td>
</tr>
<tr>
<td>Avg. all</td>
<td>Restart</td>
<td>Unowned</td>
<td>1416</td>
<td>963</td>
</tr>
<tr>
<td>Avg. all</td>
<td>Restart</td>
<td>Dirty</td>
<td>1742</td>
<td>1520</td>
</tr>
</tbody>
</table>

Memory Bandwidth Wildfire v. Origin (Mbytes/second)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Wildfire</th>
<th>Origin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pipelined local mem BW:</td>
<td>312</td>
<td>554</td>
</tr>
<tr>
<td>Pipelined local mem BW: exclusive</td>
<td>266</td>
<td>340</td>
</tr>
<tr>
<td>Pipelined local mem BW: dirty</td>
<td>246</td>
<td>182</td>
</tr>
<tr>
<td>Total local mem BW (per node)</td>
<td>2,305</td>
<td>631</td>
</tr>
<tr>
<td>Local mem BW per proc</td>
<td>96</td>
<td>375</td>
</tr>
<tr>
<td>Aggregate total mem BW (all nodes, 112 proc)</td>
<td>10,800</td>
<td>3,908</td>
</tr>
<tr>
<td>Bisection BW per processor (112 proc)</td>
<td>9,880</td>
<td>25,000</td>
</tr>
</tbody>
</table>

E6000 v. Wildfire variations: OLTP Performance for 16 procs

- Ideal, Optimized with CMR & locality scheduling, CMR only, unoptimized, poor data placement, thin nodes (2 v. 8 / node)
E6000 v. Wildfire variations: % local memory access (within node)

- Ideal, Optimized with CMR & locality scheduling, CMR only, unoptimized, poor data placement, thin nodes (2 v. 8 / node)

E10000 v. Wildfire: Red_Black Solver 24 and 36 procs

- Greater performance due to separate busses?
  - 24 proc E6000 bus utilization 90%-100%
  - 36 proc E10000 more caches => 1.7X perf v. 1.5X procs

Wildfire CMR: Red_Black Solver

- Start with all data on 1 node:
  - 500 iterations to converge (120-180 secs);
  - what if memory allocation varied over time?

Wildfire CMR benefit:
Migration vs. Replication Red_Black Solver

- Policy Iteration Iteration Number Number
  - Migrations per needed actions to reach stabilization
  - No migration or replication
  - Migration 1.6 154 sec. 99251
  - Replication 1.6 61 sec. 98545
  - Migration + replication 1.6 151 sec. 98543 85

Wildfire Remarks

- Fat nodes (8-24 way SMP) vs. Thin nodes (2-to 4-way like Origin)
- Market shift from scientific apps to database and web apps may favor a fat-node design with 8 to 16 CPUs per node
  - Scalability up to 100 CPUs may be of interest, but "sweet spot" of server market is 10s of CPUs. No customer interest in 1000 CPU machines key part of supercomputer marketplace
  - Memory access patterns of commercial apps have less sharing => as fat-node design less dependence on exact memory allocation and data placement, perform better for apps with irregular or changing data access patterns

Embedded Multiprocessors

- EmpowerTel MXP, for Voice over IP
  - 4 MIPS processors, each with 12 to 24 KB of cache
  - 13.5 million transistors, 133 MHz
  - PCI master/slave + 100 Mbit Ethernet pipe
- Embedded Multiprocessing more popular in future as apps demand more performance
  - No binary compatibility; SW written from scratch
  - Apps often have natural parallelism: set-top box, a network switch, or a game system
  - Greater sensitivity to die cost (and hence efficient use of silicon)
Pitfall: Measuring MP performance by linear speedup v. execution time

- "linear speedup" graph of perf as scale CPUs
- Compare best algorithm on each computer
- Relative speedup - run same program on MP and uniprocessor
  - But parallel program may be slower on a uniprocessor than a sequential version
  - Or developing a parallel program will sometimes lead to algorithmic improvements, which should also benefit uni
- True speedup - run best program on each machine
- Can get superlinear speedup due to larger effective cache with more CPUs

Fallacy: Amdahl’s Law doesn’t apply to parallel computers

- Since some part linear, can’t go 100X?
- 1987 claim to break it, since 1000X speedup
  - researchers scaled the benchmark to have a data set size that is 1000 times larger and compared the uniprocessor and parallel execution times of the scaled benchmark. For this particular algorithm the sequential portion of the program was constant independent of the size of the input, and the rest was fully parallel–hence, linear speedup with 1000 processors
- Usually sequential scale with data too

Fallacy: Linear speedups are needed to make multiprocessors cost-effective

- Mark Hill & David Wood 1995 study
- Compare costs SGI uniprocessor and MP
  - Uniprocessor = $38,400 + $100 * MB
  - MP = $81,600 + $20,000 * P + $100 * MB
  - 1 GB, uni = $138k v. mp = $181k + $20k * P
- What speedup for better MP cost performance?
  - 8 proc = $341k; $341k/138k => 2.5X
  - 16 proc => need only 3.6X, or 25% linear speedup
- Even if need some more memory for MP, not linear

Fallacy: Multiprocessors are “free.”

- "Since microprocessors contain support for snooping caches, can build small-scale, bus-based multiprocessors for no additional cost”
- Need more complex memory controller (coherence) than for uniprocessor
- Memory access time always longer with more complex controller
- Additional software effort: compilers, operating systems, and debuggers all must be adapted for a parallel system

Pitfall: Scalability is almost free

- “build scalability into a multiprocessor and then simply offer the multiprocessor at any point on the scale from a small number of processors to a large number”
- Cray T3E scales to 2,048 CPUs vs 4 CPU Alpha
  - At 128 CPUs, it delivers a peak bisection BW of 38.4 GB/s, or 300 MB/s per CPU (uses Alpha microprocessor)
  - Compaq Alphaserver ES40 up to 4 CPUs and has 5.6 GB/s of interconnect BW, or 1400 MB/s per CPU
- Build apps that scale requires significantly more attention to load balance, locality, potential contention, and serial (or partly parallel) portions of program. 10X is very hard

Fallacy: Not developing the software to take advantage of, or optimize for, a multiprocessor architecture

- SGI OS protects the page table data structure with a single lock, assuming that page allocation is infrequent
- Suppose a program uses a large number of pages that are initialized at start-up
- program parallelized so that multiple processes allocate the pages
- But page allocation requires lock of page table data structure, so even an OS kernel that allows multiple threads will be serialized at initialization (even if separate processes)
Multiprocessor Conclusion

- Some optimism about future
  - Parallel processing beginning to be understood in some domains
  - More performance than that achieved with a single-chip microprocessor
  - MIPS are highly effective for multiprogrammed workloads
  - MIPS proved effective for intensive commercial workloads, such as OLTP (assuming enough I/O to be CPU-limited), DSS applications (where query optimization is critical), and large-scale, web searching applications
  - On-chip MPs appears to be growing
    1) embedded market where natural parallelism often exists an obvious alternative to faster less silicon efficient, CPU
    2) diminishing returns in high-end microprocessor encourage designers to pursue on-chip multiprocessing

Synchronization

- Why Synchronize? Need to know when it is safe for different processes to use shared data
- Issues for Synchronization:
  - Uninterruptable instruction to fetch and update memory (atomic operation):
  - User level synchronization operation using this primitive:
  - For large scale MPs, synchronization can be a bottleneck; techniques to reduce contention and latency of synchronization

Uninterruptable Instruction to Fetch and Update Memory

- Atomic exchange: interchange a value in a register for a value in memory
  - 0 => synchronization variable is free
  - 1 => synchronization variable is locked and unavailable
- Test-and-set: tests a value and sets it if the value passes the test
- Fetch-and-increment: it returns the value of a memory location and atomically increments it
  - 0 => synchronization variable is free

User Level Synchronization—Operation Using this Primitive

- Spin locks: processor continuously tries to acquire, spinning around a loop trying to get the lock
- What about MP with cache coherency?
  - Want to spin on cache copy to avoid full memory latency
  - Likely to get cache hits for such variables
- Problem: exchange includes a write, which invalidates all other copies; this generates considerable bus traffic
- Solution: start by simply repeatedly reading the variable; when it changes, then try exchange ("test and testset")

Another MP Issue: Memory Consistency Models

- What is consistency? When must a processor see the new value? e.g., seems that
  - P1: A = 0; B = 0;
  - P2: A = 1; B = 1;
  - L1: if (B == 0) ...
  - L2: if (A == 0) ...
- Impossible for both if statements L1 & L2 to be true?
- What if write invalidate is delayed & processor continues?
- Memory consistency models: what are the rules for such cases?
- Sequential consistency: result of any execution is the same as if the accesses of each processor were kept in order and the accesses among different processors were interleaved => assignments before ifs above
  - SC: delay all memory accesses until all invalidates done
Memory Consistency Model

- Schemes faster execution to sequential consistency
- Not really an issue for most programs; they are synchronized
  - A program is synchronized if all access to shared data are ordered by synchronization operations
    - write(x)
    - release(s) {unlock}
    - acquire(s) {lock}
    - read(x)
- Only those programs willing to be nondeterministic are not synchronized; “data race”: outcome f(proc. speed)
- Several Relaxed Models for Memory Consistency since most programs are synchronized; characterized by their attitude towards: RAR, WAR, RAW, WAW to different addresses