Coping with CS 252
- Students with too varied background?
  - In past, CS grad students took written prelim exams on
    undergraduate material in hardware, software, and theory
  - 1st 5 weeks reviewed background, helped 252, 262, 270
  - Prelims were dropped => some unprepared for CS 252?
- In class exam on Friday January 19 (30 mins)
  - Doesn’t affect grade, only admission into class
  - 2 grades: Admitted or audit/take CS 152 1st
  - Improve your experience if recapture common background
- Review: Chapters 1, CS 152 home page, maybe
  “Computer Organization and Design (COD)2/e”
  - Chapters 1 to 8 of COD if never took prerequisite
  - If took a class, be sure COD Chapters 2, 6, 7 are familiar
  - Copies in Bechtel Library on 2-hour reserve
- FAST review today of Pipelining, Performance,
  Caches, and Virtual Memory

Pipelining: Its Natural!
- Laundry Example
  - Ann, Brian, Cathy, Dave each have one load of clothes
    to wash, dry, and fold
  - Washer takes 30 minutes
  - Dryer takes 40 minutes
  - “Folder” takes 20 minutes

Sequential Laundry
- Sequential laundry takes 6 hours for 4 loads
- If they learned pipelining, how long would laundry take?

Pipelined Laundry
- Pipelined laundry takes 3.5 hours for 4 loads

Pipelining Lessons
- Pipelining doesn’t help latency of single task, it
  helps throughput of entire workload
- Pipeline rate limited by slowest pipeline stage
- Multiple tasks operating simultaneously
- Potential speedup = Number pipe stages
- Unbalanced lengths of pipe stages reduces speedup
- Time to “fill” pipeline and time to “drain” it
  reduces speedup
Computer Pipelines

- Execute billions of instructions, so throughput is what matters
- What is desirable in instruction sets for pipelining?
  - Variable length instructions vs. all instructions same length?
  - Memory operands part of any operation vs. memory operands only in loads or stores?
  - Register operand many places in instruction format vs. registers located in same place?

A "Typical" RISC

- 32-bit fixed format instruction (3 formats)
- Memory access only via load/store instructions
- 32 32-bit GPR (R0 contains zero, DP take pair)
- 3-address, reg-reg arithmetic instruction; registers in same place
- Single address mode for load/store: base + displacement
- no indirection
- Simple branch conditions
- Delayed branch

Example: MIPS (Note register location)

5 Steps of MIPS Datapath

Visualizing Pipelining
Its Not That Easy for Computers

- Limits to pipelining: Hazards prevent next instruction from executing during its designated clock cycle
  - Structural hazards: HW cannot support this combination of instructions (single person to fold and put clothes away)
  - Data hazards: Instruction depends on result of prior instruction still in the pipeline (missing sock)
  - Control hazards: Caused by delay between the fetching of instructions and decisions about changes in control flow (branches and jumps).

One Memory Port/Structural Hazards

![Diagram of Structural Hazards](image1)

Data Hazard on R1

![Diagram of Data Hazard on R1](image2)

Three Generic Data Hazards

- **Read After Write (RAW)**
  - Instr J tries to read operand before Instr I writes it
    - I: add r1, r2, r3
    - J: sub r4, r1, r3
  - Caused by a “Dependence” (in compiler nomenclature). This hazard results from an actual need for communication.

- **Write After Read (WAR)**
  - Instr J writes operand before Instr I reads it
    - J: sub r4, r1, r3
    - K: mul r6, r1, r7
  - Called an “anti-dependence” by compiler writers. This results from reuse of the name “r1”.
  - Can’t happen in MIPS 5 stage pipeline because:
    - All instructions take 5 stages, and
    - Reads are always in stage 2, and
    - Writes are always in stage 5
Three Generic Data Hazards

- **Write After Write (WAW)**
  - Instruction 1 writes operand before Instruction 2 writes it.
  - Called an "output dependence" by compiler writers.
  - Also results from the reuse of name "r1".
  - Can't happen in MIPS 5 stage pipeline because:
    - All instructions take 5 stages, and
    - Writes are always in stage 5.
  - Will see WAR and WAW in later more complicated pipes.

CS 252 Administrivia

- All assignments, lectures via WWW page:
  [http://www.cs.berkeley.edu/~patterson/252S01/](http://www.cs.berkeley.edu/~patterson/252S01/)
- 2 Quizzes (given evenings in 8th and 14th week)
- In class exam on Friday Jan 19, last 30 minutes
  - Improve 252 experience if recapture common background
  - Bring 1 sheet of paper with notes on both sides
  - Doesn’t affect grade, only admission into class
  - 2 grades: Admitted or audit/take CS 152 1st
  - Review: Chapters 1, CS 152 home page, maybe "Computer Organization and Design (COD)2/e"
  - If did take a class, be sure COD Chapters 2, 5, 6, 7 are familiar
  - Copies in Bechtel Library on 2-hour reserve

Research Paper Reading

- As graduate students, you are now researchers.
- Most information of importance to you will be in research papers.
- Ability to rapidly scan and understand research papers is key to your success.
- So: 1 paper / week in this course
  - Quick 1 paragraph summaries will be due in class
  - Will discuss papers in class
- Papers "Readings in Computer Architecture" or online
- First assignment (before Friday): Read p. 56-59 "Cramming More Components onto Integrated Circuits" by G. E. Moore, 1965 ("Moore’s Law")

Grading

- 10% Homeworks (work in pairs)
- 40% Examinations (2 Quizzes)
- 40% Research Project (work in pairs)
  - Transition from undergrad to grad student
  - Berkeley wants you to succeed, but you need to show initiative
  - Pick topic
  - Meet 3 times with faculty/TA to see progress
  - Give oral presentation
  - Give poster session
  - Written report like conference paper
- 10% Class Participation

Forwarding to Avoid Data Hazard

Figure 3.10, Page 149, CA:AQA 2e

- add r1, r2, r3
- sub r4, r1, r3
- and r6, r1, r7
- or r8, r1, r9
- xor r10, r1, r11
Data Hazard Even with Forwarding
Figure 3.12, Page 153, CA:AQA 2e

Software Scheduling to Avoid Load Hazards
Try producing fast code for
a = b + c;
d = e – f;
assuming a, b, c, d, e, and f in memory.
Slow code:

Fast code:

Control Hazard on Branches
Three Stage Stall

Example: Branch Stall Impact
• If 30% branch, Stall 3 cycles significant
• Two part solution:
  - Determine branch taken or not sooner, AND
  - Compute taken branch address earlier
• MIPS branch tests if register = 0 or ≠ 0
• MIPS Solution:
  - Move Zero test to ID/RF stage
  - Adder to calculate new PC in ID/RF stage
  - 1 clock cycle penalty for branch versus 3

Pipelined MIPS Datapath
Figure 3.22, page 183, CA:AQA 2/e

- Data stationary control
  - Local decode for each instruction phase / pipeline stage
Four Branch Hazard Alternatives

#1: Stall until branch direction is clear

#2: Predict Branch Not Taken
- Execute successor instructions in sequence
- "Squash" instructions in pipeline if branch actually taken
- Advantage of late pipeline state update
- 47% MIPS branches not taken on average
- PC+4 already calculated, so use it to get next instruction

#3: Predict Branch Taken
- 53% MIPS branches taken on average
- But haven’t calculated branch target address in MIPS
  - MIPS still incurs 1 cycle branch penalty
  - Other machines: branch target known before outcome

#4: Delayed Branch
- Define branch to take place AFTER a following instruction
- Sequential successor instruction sequential successor...
- Branch delay of length n
- 1 slot delay allows proper decision and branch target address in 5 stage pipeline
- MIPS uses this

Delayed Branch

- Where to get instructions to fill branch delay slot?
  - Before branch instruction
  - From the target address: only valuable when branch taken
  - From fall through: only valuable when branch not taken
  - Canceling branches allow more slots to be filled

- Compiler effectiveness for single branch delay slot:
  - Fills about 60% of branch delay slots
  - About 80% of instructions executed in branch delay slots useful in computation
  - About 50% (60% x 80%) of slots usefully filled

- Delayed Branch downside: 7-8 stage pipelines, multiple instructions issued per clock (superscalar)

Now, Review of Performance

Performance(X)

\[
\text{Performance}(X) = \frac{1}{\text{Execution_time}(X)}
\]

Definitions

- Performance is in units of things per sec
  - bigger is better

- If we are primarily concerned with response time
  - \( \text{performance}(x) = \frac{1}{\text{execution_time}(x)} \)

"X is n times faster than Y" means

\[
n = \frac{\text{Performance}(X)}{\text{Performance}(Y)} = \frac{\text{Execution_time}(Y)}{\text{Execution_time}(X)}
\]

Which is faster?

<table>
<thead>
<tr>
<th></th>
<th>DC-30</th>
<th>747</th>
<th>Concorde</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>6.5 h</td>
<td>610 mph</td>
<td>6.5 h</td>
</tr>
<tr>
<td>Throughput</td>
<td></td>
<td>286,700</td>
<td></td>
</tr>
</tbody>
</table>

- Time to run the task (ExTime)
  - Execution time, response time, latency

- Tasks per day, hour, week, sec ... (Performance)
  - Throughput, bandwidth
Aspects of CPU Performance (CPU Law)

<table>
<thead>
<tr>
<th>CPU time</th>
<th>Seconds</th>
<th>Instructions</th>
<th>Cycles</th>
<th>Seconds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compiler</td>
<td>X</td>
<td>(X)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inst. Set.</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organization</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Cycles Per Instruction (Throughput)

"Average Cycles per Instruction"

\[ \text{CPI} = \frac{\text{CPU Time} \times \text{Clock Rate}}{\text{Instruction Count}} \]

"Instruction Frequency"

\[ \text{CPI} = \sum_{i} \frac{f_i}{N} \times \frac{I_i}{n} \quad \text{where} \quad f_i = \frac{I_i}{\text{Instruction Count}} \]

Example: Calculating CPI

<table>
<thead>
<tr>
<th>Base Machine (Reg / Reg)</th>
<th>Op</th>
<th>Freq</th>
<th>Cycles</th>
<th>CPI(i)</th>
<th>(% Time)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>50%</td>
<td>1</td>
<td>.5</td>
<td>(33%)</td>
<td></td>
</tr>
<tr>
<td>Load</td>
<td>20%</td>
<td>2</td>
<td>.4</td>
<td>(27%)</td>
<td></td>
</tr>
<tr>
<td>Store</td>
<td>10%</td>
<td>2</td>
<td>.2</td>
<td>(13%)</td>
<td></td>
</tr>
<tr>
<td>Branch</td>
<td>20%</td>
<td>2</td>
<td>1.5</td>
<td>(27%)</td>
<td></td>
</tr>
</tbody>
</table>

Example: Branch Stall Impact

- Assume CPI = 1.0 ignoring branches
- Assume solution was stalling for 3 cycles
- If 30% branch, Stall 3 cycles

- Op  Freq  Cycles  CPI(i)  (% Time)
- Other 70% 1 .7 (37%)
- Branch 30% 4 1.2 (63%)

⇒ new CPI = 1.9, or almost 2 times slower

Example 2: Speed Up Equation for Pipelining

\[ \text{CPI}_{\text{pipelined}} = \text{Ideal CPI} + \text{Average Stall cycles per Inst} \]

\[ \text{Speedup} = \frac{\text{Ideal CPI} \times \text{Pipeline depth}}{\text{Ideal CPI} \times \text{Pipeline stall CPI} \times \text{Cycle Time}_{\text{pipeline}}} \times \frac{\text{Cycle Time}_{\text{pipeline}}}{\text{Cycle Time}_{\text{pipeline}}} \]

For simple RISC pipeline, CPI = 1:

\[ \text{Speedup} = \frac{\text{Pipeline depth}}{1 + \text{Pipeline stall CPI} \times \text{Cycle Time}_{\text{pipeline}}} \times \frac{\text{Cycle Time}_{\text{pipeline}}}{\text{Cycle Time}_{\text{pipeline}}} \]

Example 3: Evaluating Branch Alternatives (for 1 program)

<table>
<thead>
<tr>
<th>Schedule</th>
<th>Branch scheme</th>
<th>CPI speedup v. stall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stall</td>
<td>3 1.42</td>
<td>1.0</td>
</tr>
<tr>
<td>Predict taken</td>
<td>1 1.14</td>
<td>1.26</td>
</tr>
<tr>
<td>Predict not taken</td>
<td>1 1.09</td>
<td>1.29</td>
</tr>
<tr>
<td>Delayed branch</td>
<td>0.5 1.07</td>
<td>1.31</td>
</tr>
</tbody>
</table>

Conditional & Unconditional = 14%, 65% change PC
Example 4: Dual-port vs. Single-port

- Machine A: Dual ported memory ("Harvard Architecture")
- Machine B: Single ported memory, but its pipelined implementation has a 1.05 times faster clock rate
- Ideal CPI = 1 for both
- Loads are 40% of instructions executed

\[
\text{SpeedUp}_A = \frac{\text{Pipeline Depth}}{1 + 0} \times \frac{\text{clock}_{\text{unpipe}}}{\text{clock}_{\text{pipe}}} = \text{Pipeline Depth}
\]

\[
\text{SpeedUp}_B = \frac{\text{Pipeline Depth}}{1 + 0.4 \times 1} \times \left(\frac{\text{clock}_{\text{unpipe}}}{\text{clock}_{\text{unpipe}} / 1.05}\right) = \frac{\text{Pipeline Depth}}{1.4} \times 1.05 = 0.75 \times \text{Pipeline Depth}
\]

\[
\text{SpeedUp}_A / \text{SpeedUp}_B = \frac{\text{Pipeline Depth}}{0.75 \times \text{Pipeline Depth}} = 1.33
\]

- Machine A is 1.33 times faster

Recap: Who Cares About the Memory Hierarchy?

Processor-DRAM Memory Gap (latency)

<table>
<thead>
<tr>
<th>Year</th>
<th>Processor Performance Growth (grows 50% / year)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1982</td>
<td>100s bytes</td>
</tr>
<tr>
<td>1983</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1984</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1985</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1986</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1987</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1988</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1989</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1990</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1991</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1992</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1993</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1994</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1995</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1996</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1997</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1998</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>1999</td>
<td>9%/yr.</td>
</tr>
<tr>
<td>2000</td>
<td>9%/yr.</td>
</tr>
</tbody>
</table>

Levels of the Memory Hierarchy

- **Hit**:
  - Data appears in some block in the upper level (example: Block X)
  - Hit Rate: the fraction of memory access found in the upper level
  - Hit Time: Time to access the upper level which consists of RAM access time + Time to determine hit/miss
- **Miss**:
  - Data needs to be retrieved from a block in the lower level (Block Y)
  - Miss Rate = 1 - Hit Rate
  - Miss Penalty: Time to replace a block in the upper level + Time to deliver the block to the processor

The Principle of Locality

- **The Principle of Locality**:
  - Program access a relatively small portion of the address space at any instant of time.
- **Two Different Types of Locality**:
  - **Temporal Locality** (Locality in Time): If an item is referenced, it will tend to be referenced again soon (e.g., loops, reuse)
  - **Spatial Locality** (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon (e.g., straight-line code, array access)
- **Last 15 years, HW (hardware) relied on locality for speed**

Memory Hierarchy: Terminology

- **Hit Rate**: the fraction of memory access found in the upper level
- **Hit Time**: Time to access the upper level which consists of RAM access time + Time to determine hit/miss
- **Miss Rate**: 1 - Hit Rate
- **Miss Penalty**: Time to replace a block in the upper level + Time to deliver the block to the processor

- **Hit Time << Miss Penalty** (500 instructions on 21264)

---

Now, Review of Memory Hierarchy
Cache Measures

- **Hit rate**: fraction found in that level
  - So high that usually talk about **Miss rate**
  - Miss rate fidelity: as MIPS to CPU performance, miss rate to average memory access time in memory
- **Average memory-access time**
  - Hit time + Miss rate x Miss penalty (ns or clocks)
- **Miss penalty**: time to replace a block from lower level, including time to replace in CPU
  - *access time*: time to lower level
  - *transfer time*: time to transfer block
    - = f(BW between upper & lower levels)

1 KB Direct Mapped Cache, 32B blocks

- For a 2 ** N byte cache:
  - The uppermost (32 - N) bits are always the Cache Tag
  - The lowest M bits are the Byte Select (Block Size = 2 ** M)

Disadvantage of Set Associative Cache

- **N-way Set Associative Cache v. Direct Mapped Cache**:
  - *N* comparators vs. 1
  - Extra MUX delay for the data
  - Data comes AFTER Hit/Miss
- **In a direct mapped cache, Cache Block is available BEFORE Hit/Miss**:
  - Possible to assume a hit and continue. Recover later if miss.

4 Questions for Memory Hierarchy

- Q1: Where can a block be placed in the upper level? (Block placement)
- Q2: How is a block found if it is in the upper level? (Block identification)
- Q3: Which block should be replaced on a miss? (Block replacement)
- Q4: What happens on a write? (Write strategy)
Q1: Where can a block be placed in the upper level?

- Block 12 placed in 8 block cache:
  - Fully associative, direct mapped, 2-way set associative
  - S.A. Mapping = Block Number Modulo Number Sets

<table>
<thead>
<tr>
<th>Cache</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>01234567</td>
<td>01234567</td>
</tr>
<tr>
<td>01234567</td>
<td>01234567</td>
</tr>
<tr>
<td>01234567</td>
<td>01234567</td>
</tr>
</tbody>
</table>

Q2: How is a block found if it is in the upper level?

- Tag on each block
  - No need to check index or block offset
- Increasing associativity shrinks index, expands tag

<table>
<thead>
<tr>
<th>Block Address</th>
<th>Tag</th>
<th>Index</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Q3: Which block should be replaced on a miss?

- Easy for Direct Mapped
- Set Associative or Fully Associative:
  - Random
  - LRU (Least Recently Used)

<table>
<thead>
<tr>
<th>Assoc: 2-way</th>
<th>4-way</th>
<th>8-way</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>LRU</td>
<td>Ran</td>
</tr>
<tr>
<td>16 KB</td>
<td>5.2%</td>
<td>5.7%</td>
</tr>
<tr>
<td>64 KB</td>
<td>1.9%</td>
<td>2.0%</td>
</tr>
<tr>
<td>256 KB</td>
<td>1.15%</td>
<td>1.17%</td>
</tr>
</tbody>
</table>

Q4: What happens on a write?

- Write through—The information is written to both the block in the cache and to the block in the lower-level memory.
- Write back—The information is written only to the block in the cache. The modified cache block is written to main memory only when it is replaced.
  - Is block clean or dirty?
- Pros and Cons of each?
  - WT: read misses cannot result in writes
  - WB: no repeated writes to same location
- WT always combined with write buffers so that don’t wait for lower level memory

A Modern Memory Hierarchy

- By taking advantage of the principle of locality:
  - Present the user with as much memory as is available in the cheapest technology.
  - Provide access at the speed offered by the fastest technology.

By using the principle of locality, the memory hierarchy is organized to provide fast access to frequently used data while minimizing the cost of storage. This is achieved by using a combination of high-speed on-chip caches and lower-speed off-chip memory. The hierarchy includes:

- Processor: central processing unit
- Registers: temporary storage locations
- Main Memory: primary storage
  - DRAM: dynamic random-access memory
- Second Level Cache: faster than main memory
- Tertiary Storage: secondary storage (disk/tape)

The hierarchy is designed to balance cost and performance, with the fastest technology at the top of the hierarchy and the slowest at the bottom. This allows for efficient memory management and data access.
Summary #1/4: Pipelining & Performance

- Just overlap tasks; easy if tasks are independent
- Speed Up $\leq$ Pipeline Depth; if ideal CPI is 1, then:
  \[ \text{Speedup} = \frac{\text{Pipeline depth}}{\text{Cycle Time}_{\text{pipeline}}} \times \frac{\text{Cycle Time}_{\text{pipeline}}}{\text{Cycle Time}} \]
- Hazards limit performance on computers:
  - Structural: need more HW resources
  - Data (RAW, WAR, WAW): need forwarding, compiler scheduling
  - Control: delayed branch, prediction
- Time is measure of performance: latency or throughput
- CPI Law:

<table>
<thead>
<tr>
<th>CPU time x Seconds</th>
<th>Instructions x Cycles x Seconds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program</td>
<td>Program</td>
</tr>
<tr>
<td>Instruction</td>
<td>Instruction</td>
</tr>
<tr>
<td>Cycle</td>
<td>Cycle</td>
</tr>
</tbody>
</table>

Summary #2/4: Caches

- The Principle of Locality:
  - Program access a relatively small portion of the address space at any instant of time.
  - Temporal Locality: Locality in Time
  - Spatial Locality: Locality in Space
- Three Major Categories of Cache Misses:
  - Compulsory Misses: sad facts of life. Example: cold start misses.
  - Capacity Misses: increase cache size
  - Conflict Misses: increase cache size and/or associativity.
- Write Policy:
  - Write Through: needs a write buffer
  - Write Back: control can be complex
- Today CPU time is a function of (ops, cache misses) vs. just f(ops): What does this mean to Compilers, Data structures, Algorithms?

Summary #3/4: The Cache Design Space

- Several interacting dimensions:
  - cache size
  - block size
  - associativity
  - replacement policy
  - write-through vs write-back
- The optimal choice is a compromise:
  - depends on access characteristics
  - use (I-cache, D-cache, TLB)
  - depends on technology / cost
- Simplicity often wins

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Associativity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bad</td>
<td>More</td>
</tr>
<tr>
<td>Good</td>
<td>Less</td>
</tr>
</tbody>
</table>

Review #4/4: TLB, Virtual Memory

- Caches, TLBs, Virtual Memory all understood by examining how they deal with 4 questions: 1) Where can block be placed? 2) How is block found? 3) What block is replaced on miss? 4) How are writes handled?
- Page tables map virtual address to physical address
- TLBs make virtual memory practical
  - Locality in data => locality in addresses of data, temporal and spatial
- TLB misses are significant in processor performance
  - funny times, as most systems can't access all of 2nd level cache without TLB misses!
- Today VM allows many processes to share single memory without having to swap all processes to disk; today VM protection is more important than memory hierarchy.