The Evolution of DSP Processors

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Outline

- DSP applications
- Digital filtering as a motivating problem
- The first generation of DSPs, with an example
- Comparison of DSP processors to general-purpose processors
- DSP evolution continues... later-generation DSPs and alternatives
- Conclusions

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Who Cares?

- DSP is a key enabling technology for many types of electronic products
- DSP-intensive tasks are the performance bottleneck in many computer applications today
- Computational demands of DSP-intensive tasks are increasing very rapidly
- In many embedded applications, general-purpose microprocessors are not competitive with DSP-oriented processors today
- 1997 market for DSP processors: $3 billion

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Example DSP Applications

- Digital cellular phones
- Automated inspection
- Vehicle collision avoidance
- Voice over Internet
- Motor control
- Consumer audio
- Voice mail
- Navigation equipment
- Audio production
- Videoconferencing
- Pagers
- Music synthesis, effects
- Satellite communications
- Seismic analysis
- Secure communications
- Tapeless answering machines
- Sonar
- Cordless phones
- Digital cameras
- Modems (POTS, ISDN, cable,...)
- Noise cancellation
- Medical ultrasound
- Patient monitoring
- Radar

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Today's DSP "Killer Apps"

In terms of dollar volume, the biggest markets for DSP processors today include:

- **Digital cellular telephony**
- **Pagers and other wireless systems**
- **Modems**
- **Disk drive servo control**

  - **Most demand good performance**
  - **All demand low cost**
  - **Many demand high energy efficiency**

Trends are towards better support for these (and similar) major applications.

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DSP Tasks for Microprocessors

- Speech and audio compression
- Filtering
- Modulation and demodulation
- Error correction coding and decoding
- Servo control
- Audio processing (e.g., surround sound, noise reduction, equalization, sample rate conversion, echo cancellation)
- Signaling (e.g., DTMF detection)
- Speech recognition
- Signal synthesis (e.g., music, speech synthesis)

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What Do DSP Processors Need to Do Well?

Most DSP tasks require:

- **Repetitive numeric computations**
- **Attention to numeric fidelity**
- **High memory bandwidth, mostly via array accesses**
- **Real-time processing**

Processors must perform these tasks efficiently while minimizing:

- **Cost**
- **Power**
- **Memory use**
- **Development time**

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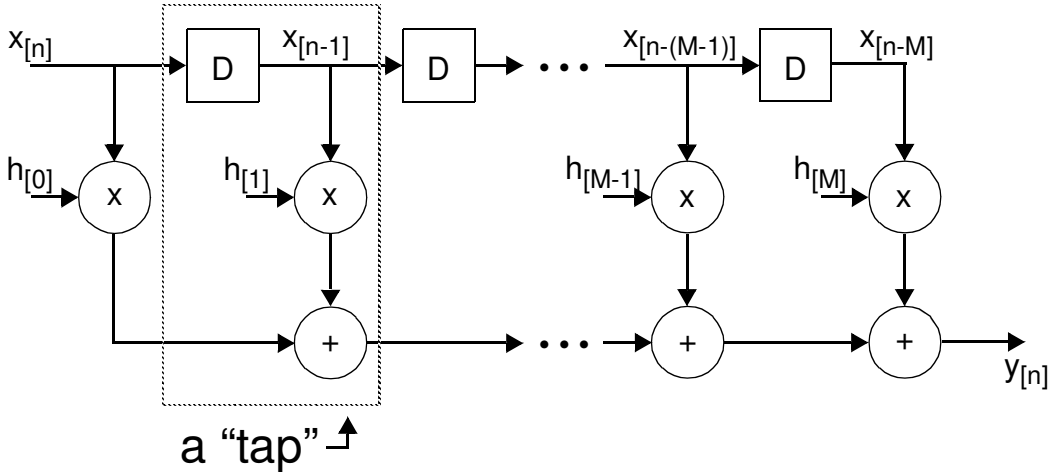
FIR Filtering: A Motivating Problem



Each tap (M+1 taps total) nominally requires:

- **Two data fetches**
- **Multiply**
- **Accumulate**
- **Memory write-back to update delay line**

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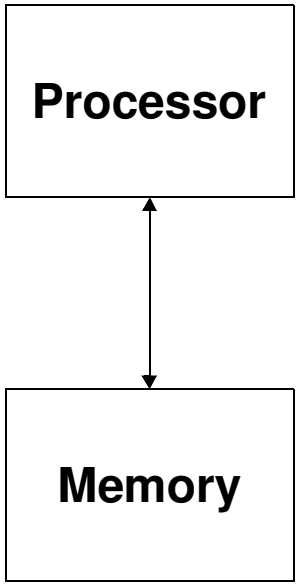
FIR Filter on Von Neumann Architecture

```
loop:

    mov     *r0,x0
    mov     *r1,y0
    mpy     x0,y0,a
    add     a,b
    mov     y0,*r2
    inc     r0
    inc     r1
    inc     r2
    dec     ctr
    tst     ctr
    jnz     loop
```



Problems: Bus / memory bandwidth bottleneck, control code overhead

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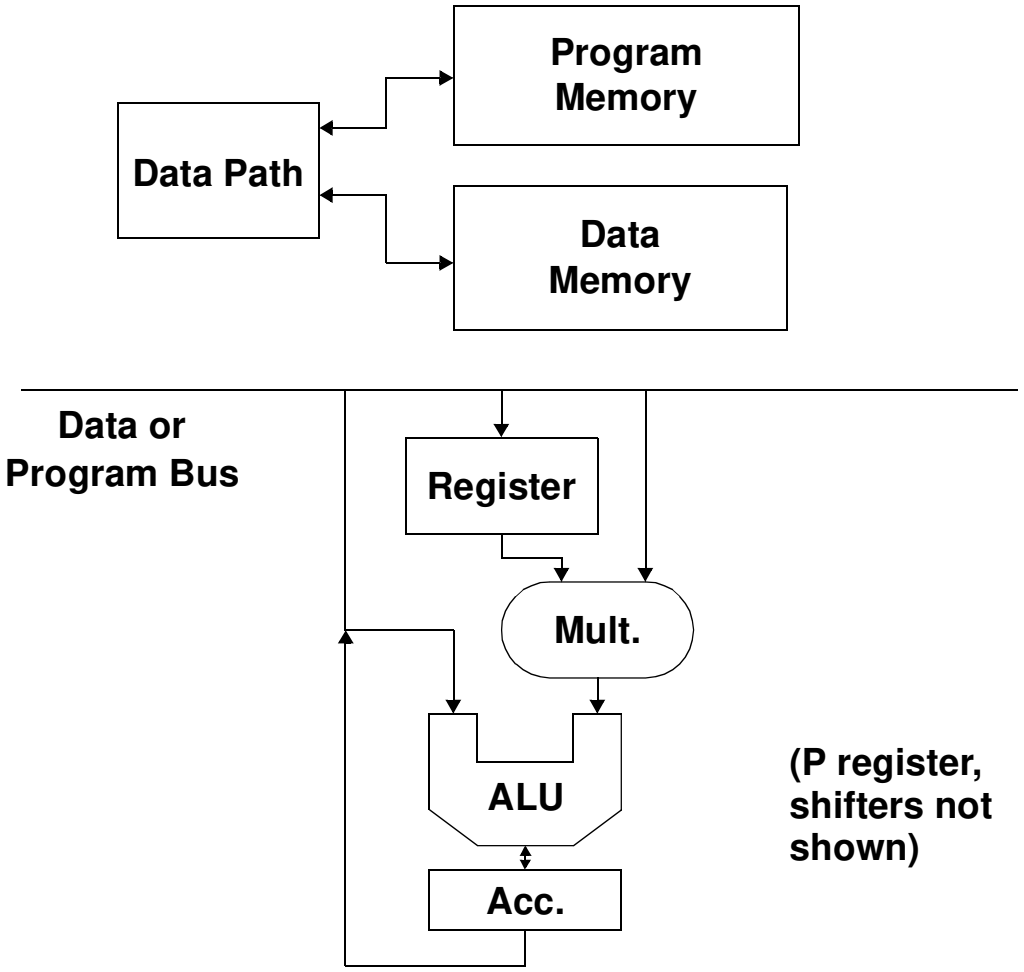
First Generation DSP (1982): Texas Instruments TMS32010

- 16-bit fixed-point
- Harvard architecture
- Accumulator
- Specialized instruction set
- 390 ns MAC time (228 ns today)



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TMS32010 FIR Filter Code

Here X4, H4, etc. are direct (absolute) memory addresses:

```
LT     X4        ; Load T with x(n-4)
MPY    H4        ; P = H4*X4

LTD    X3        ; Load T with x(n-3); x(n-4) = x(n-3);
                 ; Acc = Acc + P
MPY    H3        ; P = H3*X3

LTD    X2
MPY    H2

etc.
```

- **Two instructions per tap, but requires unrolling**

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Features Common to Most DSP Processors

- Data path configured for DSP
- Specialized instruction set
- Multiple memory banks and buses
- Specialized addressing modes
- Specialized execution control
- Specialized peripherals for DSP

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Data Path

DSP Processor

- Specialized hardware performs all key arithmetic operations in 1 cycle.
- Hardware support for managing numeric fidelity:
  - Shifters
  - Guard bits
  - Saturation

General-Purpose Processor

- Multiplies often take >1 cycle
- Shifts often take >1 cycle
- Other operations (e.g., saturation, rounding) typically take multiple cycles

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Instruction Set

DSP Processor

- Specialized, complex instructions
- Multiple operations per instruction

```
mac x0,y0,a   x:(r0)+,x0   y:(r4)+,y0
```

General-Purpose Processor

- General-purpose instructions
- Typically only one operation per instruction

```
mov *r0,x0
mov *r1,y0
mpy x0,y0,a
add a,b
mov y0,*r2
inc r0
inc r1
```


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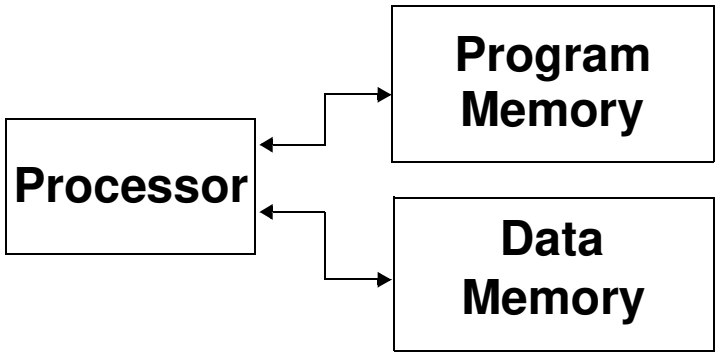
Memory Architecture

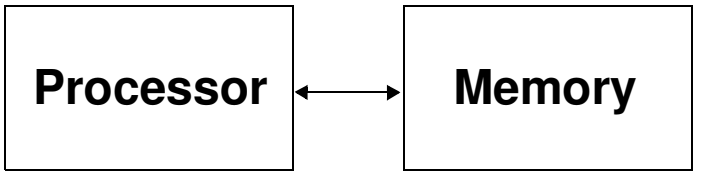
DSP Processor

- Harvard architecture
- 2-4 memory accesses/ cycle
- No caches—on-chip SRAM

General-Purpose Processor

- Von Neumann architecture
- Typically 1 access/ cycle
- May use caches





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Addressing

DSP Processor

- Dedicated address generation units
- Specialized addressing modes; e.g.:
  - Autoincrement
  - Modulo (circular)
  - Bit-reversed (for FFT)
- Good immediate data support

General-Purpose Processor

- Often, no separate address generation unit
- General-purpose addressing modes

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Execution Control

- Hardware support for fast looping
- “Fast interrupts” for I/O handling
- Real-time debugging support

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Specialized Peripherals for DSPs

- Synchronous serial ports
- Parallel ports
- Timers
- On-chip A/D, D/A converters
- Host ports
- Bit I/O ports
- On-chip DMA controller
- Clock generators

- On-chip peripherals often designed for “background” operation, even when core is powered down.

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