CS152
Computer Architecture and Engineering
Notes to Lecturers Using Notes

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lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/

Overview of notes for lecturers

- Fall 1997 Lecture Schedule
- Things that worked well
- Things would change for next time

Schedule from Fall '97 CS152

Date	*Lecture*	*File name*	*Topic/Title*
8/27	#1	lec01-intro	Introduction; 5 components of a computer
8/29	#2	lec02-isareview	Review of MIPS ISA, Performance
9/3	#3	lec03-delay	Review of Technology, Delay Modeling
9/5	#4		Prerequisite Quiz
9/10	#5	lec05-cost	Cost and Design
9/12	#6	lec06-mult	The Design Process,Multiply
9/19	#7	lec07-div-fp	Divide, FP Numbers,Pentium bug
9/24	#8	lec08-single	Designing a Single Cycle Datapath
9/26	#9	lec09-single.control	Designing Single Cycle Control
10/1	#10	lec10-muticycle	Designing a Multiple Cycle Processor
10/3	#11	lec11-micro	Microprogramming and exceptions
10/10	#12	lec12-micro	Designing a Multiple Cycle Controller and Exceptions
10/17		low_power.ps	Low Power (Prof. Brodersen)
10/19	#13	lec13-pipelining	Pipelining Intro
10/22	#14	lec14-pipelining-adv	Pipelining Control and Exceptions
10/24	#15	lec15-pipelining-3	Advanced Pipelinging
10/29	#16	lec16-memory	Introduction to Memory System Design
10/31	#17	lec17-cache	Cache and Virtual Memory
11/5	#18	io.ps	I/O Devices and Systems (Brian Wong, Sun)
11/7	#19		I/O Devices and Systems 2 (Brian Wong, Sun)
11/12	#20	CS152_dsp.pdf	DSP Design I (Prof. Brodersen)
11/14	#21	slides.evolution.ps	DSP Design II (Jeff Bier, BDTI)
11/26	#24	lec20-badtalk	How to Give a Bad Talk + SPARC 10th Anniversary Video
12/5	#25	lec25-final	Course Overview, lessons for CS152, your Cal legacy

Things that worked well

- Prerequisite Quiz
  - Surveyed class, 34/37 thought it was a good idea, 2/37 OK, 1/37 bad
  - Since there are 2 prerequisites (logic design and machine organization), even if they took logic design prior semester (which not all did), machine organization might have been a long time ago, and may not have had MIPS. Saved time and brought everyone up to speed
- How to Give a Bad Talk
  - Spending 30 minutes telling them the difference between good and bad talks, and the importance of practice, really paid off during 30 minute oral presentations of projects
- Basic flow of lectures and labs
  - This time the lectures were close to the time of the labs, vs. getting too far ahead
  - Putting an occasional guest lecture helped keep timing synched

Things that worked well, II

- Online lectures
  - Popular with class
  - In total over 1000 slides (more slides than pages of COD 2/e!)
  - Need to be careful not to race through slides in last 30 minutes to catch up; just take off from next time
  - Connecting what's in class to what's going on in industry
- Field Trip
  - Popular; would have liked to see a fab line next time
- Spread out midterms
  - Gave us time to prepare midterms in leasurely fashion
- Old midterms AND SOLUTIONS online
  - Let students review material by testing themselves, see what don't understand
  - Its a way to trick students into learning more by figuring out 16 or so hard problems on their own

Things that worked well, III

- Basic flow of lectures, labs, and projects
  - ALU -> single cycle datapath -> pipelined datapath -> cache
  - Every project did some extra credit, got pipelined machine working (What was Award winning dissertation in 1984 is undergrad project in 1997!)
  - Nice that had more freedom on what to do in cache design
  - Also, since cache was a new piece, it allowed them use lessons learned from datapath mistakes
- 2 weeks per lab assignment
  - Giving 3 weeks didn't help in Fall '95, since most just postponed
  - Also allowed things to slip without disastrous consequences
    - Perhaps add a buffer to assume something will slip (e.g., 3 weeks between Lab 4 and Lab 5)?
  - Virtually everyone was done before Thanksgiving, just doing extra credit and project
- 2 hour labs, all teammates in same lab section
  - Giving oral presentation during lab slot simplified scheduling
  - Time for them to meet to discuss projects

Things would change for next time

- Lecure #3 is not really a review; critical timing stuff is new to most of them, move some material out
- Some question as to whether should have moved multiply, divide, floating point (lectures #6 and #7) into prerequisite quiz and freeed up time for later
- Lecture #11 (lec11-micro)
  - This was based on datapath of 1st edition of book (changed in 2nd edtion) and was very confusing to the class. I fixed the datapath in the following lecture (lec12-micro). I would throw out most of 11 and replace with 12.

Things would change for next time

- Add lecture on VHDL
  - There is a short piece now. Culler had slides in F96 version (lec07-vhdl, lec10-proc-vhdl) so I would include that material
  - I was sick and missed a lecture (9/17), so there is room
  - Student problems on project due to VHDL:
    - Not creating and following a consistent naming convention so that can put independent modules together
    - Didn't realize that number at end of name (A4) can result in VHDL treating singal as a bus (A is 4 bits wide)
    - Reordering the list of signal pins can change behavior of module, even though it shouldn't
- Perhaps turn lectures #16 and #17 on memory, caches, TLB, virtual memory into 3 lectures?
  - Try to avoid duplicating what's in OS courses, concentrating on HW pieces and consequences (TLB, restarting instructions)

Things would change for next time, II

- Lecture #17 and #18 on I/O
  - Brian Wong was an interesting guest lecturer, but we need 1 or 2 real lectures on busses and I/O.
  - I would use lectures from before from either Fall 96 Culler (lec20-bus, lec21-IO) or from me in Fall 95 (lecture19 IO)
- Amazingly, students don't check their online scores to be sure there are no missing entries or mistakes even if told to do so a few times
  - Perhaps require them to print out grades thus far and turn them in with project?
  - Get TAs to enter all scores intro spreadsheet on day project and send email to students is due if have missing scores?
- Large groups: 5 seemed much harder than 4, but they learned value of management
  - Perhaps randomly assign students next time to avoid homogeneous race teams (all indian, all pacific islander, ...)?
- Might add a guest lecture on managing projects?

Things would change for next time, III

- Having all grad students as TAs would was nice, but none had taken the class. Would be helpful to have at least one undergrad TA (even at 10 hours) in the mix so that can have an experience base to include in our discussions on assignments, how logic blocks worked (is the read line a level or a pulse?).
  - Perhaps he would help with large discussion section, given roving office hour responsibilities, or responsible for revising labs to make them clearer?
  - Could even pay from own funds. Cost is some like 10 hours/ week * 16 weeks * $11/hour or < $2000

New Ideas

- Dr. Ed Gehringer (efg@ncsu.edu) at North Carolina State University has developed a database of Computer Architecture course materials on the World Wide Web
- It contains approximately two hundred questions from Computer Architecture course assignments at different universities
- It wasn't available in time to use, but might want to try using it to get ideas for quizzes, homeworks; also to contribute problems to keep such a noble effort alive
- Need to send him email to get the password