CS152
Computer Architecture and Engineering
Lecture 2

August 29, 1997
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lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/
Overview of Today’s Lecture: Review Instruction Sets, Performance

° Review from Last Lecture (1 minute)
° Classes, Addressing, Format (20 minutes)
° Administrative Matters (3 minutes)
° Operations, Branching, Calling conventions (25 minutes)
° Break (5 minutes)
° MIPS Details, Performance (25 minutes)
Review: Organization

° All computers consist of five components
  • Processor: (1) datapath and (2) control
  • (3) Memory
  • (4) Input devices and (5) Output devices

° Not all “memory” are created equally
  • Cache: fast (expensive) memory are placed closer to the processor
  • Main memory: less expensive memory—we can have more

° Input and output (I/O) devices have the messiest organization
  • Wide range of speed: graphics vs. keyboard
  • Wide range of requirements: speed, standard, cost ...
  • Least amount of research (so far)
Summary: Computer System Components

- Proc
- Caches
- Busses
- Memory
- I/O Devices:
  - Controllers
  - Disks
  - Displays
  - Keyboards
  - Networks

° All have interfaces & organizations
Review: Instruction Set Design

Which is easier to change?
Instruction Set Architecture: What Must be Specified?

- Instruction Format or Encoding
  - how is it decoded?

- Location of operands and result
  - where other than memory?
  - how many explicit operands?
  - how are memory operands located?
  - which can or cannot be in memory?

- Data type and Size

- Operations
  - what are supported

- Successor instruction
  - jumps, conditions, branches
  - *fetch-decode-execute is implicit!*
Basic ISA Classes

Accumulator (1 register):

1 address add A acc ← acc + mem[A]
1+x address addx A acc ← acc + mem[A + x]

Stack:

0 address add tos ← tos + next

General Purpose Register:

2 address add A B EA(A) ← EA(A) + EA(B)
3 address add A B C EA(A) ← EA(B) + EA(C)

Load/Store:

3 address add Ra Rb Rc Ra ← Rb + Rc
  load Ra Rb Ra ← mem[Rb]
  store Ra Rb mem[Rb] ← Ra

Comparison:

Bytes per instruction? Number of Instructions? Cycles per instruction?
Comparing Number of Instructions

° Code sequence for $C = A + B$ for four classes of instruction sets:

<table>
<thead>
<tr>
<th>Stack</th>
<th>Accumulator</th>
<th>Register (register-memory)</th>
<th>Register (load-store)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Push A</td>
<td>Load A</td>
<td>Load R1,A</td>
<td>Load R1,A</td>
</tr>
<tr>
<td>Push B</td>
<td>Add B</td>
<td>Add R1,B</td>
<td>Load R2,B</td>
</tr>
<tr>
<td>Add</td>
<td>Store C</td>
<td>Store C, R1</td>
<td>Add R3,R1,R2</td>
</tr>
<tr>
<td>Pop C</td>
<td></td>
<td></td>
<td>Store C,R3</td>
</tr>
</tbody>
</table>
General Purpose Registers Dominate

- 1975-1995 all machines use general purpose registers

- Advantages of registers
  - registers are faster than memory
  - registers are easier for a compiler to use
    - e.g., \((A*B) - (C*D) - (E*F)\) can do multiplies in any order vs. stack
  - registers can hold variables
    - memory traffic is reduced, so program is sped up (since registers are faster than memory)
    - code density improves (since register named with fewer bits than memory location)
Summary on Instruction Classes

- Expect new instruction set architecture to use general purpose register
- Pipelining => Expect it to use load store variant of GPR ISA
MIPS I Registers

- Programmable storage
  - $2^{32}$ x bytes of memory
  - 31 x 32-bit GPRs ($R0 = 0$)
  - 32 x 32-bit FP regs (paired DP)
  - HI, LO, PC
Memory Addressing

° Since 1980 almost every machine uses addresses to level of 8-bits (byte)

° 2 questions for design of ISA:
  • Since could read a 32-bit word as four loads of bytes from sequential byte addresses or as one load word from a single byte address, how do byte addresses map onto words?
  • Can a word be placed on any byte boundary?
Addressing Objects: Endianess and Alignment

- **Big Endian:** address of most significant byte = word address (xx00 = Big End of word)
  - IBM 360/370, Motorola 68k, MIPS, Sparc, HP PA

- **Little Endian:** address of least significant byte = word address (xx00 = Little End of word)
  - Intel 80x86, DEC Vax, DEC Alpha (Windows NT)

Alignment: require that objects fall on an address that is multiple of their size.
## Addressing Modes

<table>
<thead>
<tr>
<th>Addressing mode</th>
<th>Example</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>Add R4,R3</td>
<td>R4 ← R4+R3</td>
</tr>
<tr>
<td>Immediate</td>
<td>Add R4,#3</td>
<td>R4 ← R4+3</td>
</tr>
<tr>
<td>Displacement</td>
<td>Add R4,100(R1)</td>
<td>R4 ← R4+Mem[100+R1]</td>
</tr>
<tr>
<td>Register indirect</td>
<td>Add R4,(R1)</td>
<td>R4 ← R4+Mem[R1]</td>
</tr>
<tr>
<td>Indexed / Base</td>
<td>Add R3,(R1+R2)</td>
<td>R3 ← R3+Mem[R1+R2]</td>
</tr>
<tr>
<td>Direct or absolute</td>
<td>Add R1,(1001)</td>
<td>R1 ← R1+Mem[1001]</td>
</tr>
<tr>
<td>Memory indirect</td>
<td>Add R1,@(R3)</td>
<td>R1 ← R1+Mem[Mem[R3]]</td>
</tr>
<tr>
<td>Auto-increment</td>
<td>Add R1,(R2)+</td>
<td>R1 ← R1+Mem[R2]; R2 ← R2+d</td>
</tr>
<tr>
<td>Auto-decrement</td>
<td>Add R1,–(R2)</td>
<td>R2 ← R2–d; R1 ← R1+Mem[R2]</td>
</tr>
<tr>
<td>Scaled</td>
<td>Add R1,100(R2)[R3]</td>
<td>R1 ← R1+Mem[100+R2+R3*d]</td>
</tr>
</tbody>
</table>

*Why Auto-increment/decrement? Scaled?*
Addressing Mode Usage? (ignore register mode)
3 programs measured on machine with all address modes (VAX)

--- Displacement: 42% avg, 32% to 55% 75%
--- Immediate: 33% avg, 17% to 43% 85%
--- Register deferred (indirect): 13% avg, 3% to 24%
--- Scaled: 7% avg, 0% to 16%
--- Memory indirect: 3% avg, 1% to 6%
--- Misc: 2% avg, 0% to 3%

75% displacement & immediate
88% displacement, immediate & register indirect
Displacement Address Size?

- Avg. of 5 SPECint92 programs v. avg. 5 SPECfp92 programs
- X-axis is in powers of 2: 4 => addresses > $2^3$ (8) and $\leq 2^4$ (16)
- 1% of addresses > 16-bits
- 12 - 16 bits of displacement needed
Immediate Size?

- 50% to 60% fit within 8 bits
- 75% to 80% fit within 16 bits
Addressing Summary

• Data Addressing modes that are important: Displacement, Immediate, Register Indirect

• Displacement size should be 12 to 16 bits

• Immediate size should be 8 to 16 bits
Generic Examples of Instruction Format Widths

Variable:

Fixed:

Hybrid:
Summary of Instruction Formats

• If code size is most important, use variable length instructions

• If performance is over is most important, use fixed length instructions

• Recent embedded machines (ARM, MIPS) added optional mode to execute subset of 16-bit wide instructions (Thumb, MIPS16); per procedure decide performance or density
Instruction Format

• If have many memory operands per instructions and many addressing modes,
  => Address Specifier per operand

• If have load-store machine with 1 address per instr. and one or two addressing modes,
  => encode addressing mode in the opcode
MIPS Addressing Modes/Instruction Formats

- All instructions 32 bits wide

Register (direct)

Immediate

Base+index

PC-relative

• Register Indirect?
Administrative Matters

CS152 news group: ucb.class.cs152 (email patterson@cs with specific questions)

• Slides, handouts available via WWW: http://www-inst.eecs.berkeley.edu/~cs152/fa97

° Video tapes of lectures available for viewing in 205 McLaughlin

• Prerequisite quiz Friday September 5: CS 61C, CS 150
• Review Chapters 1-4 of COD:HSI Second Edition
• Turn in survey forms with photo
Typical Operations (little change since 1960)

<table>
<thead>
<tr>
<th>Operation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Movement</td>
<td>Load (from memory)</td>
</tr>
<tr>
<td></td>
<td>Store (to memory)</td>
</tr>
<tr>
<td></td>
<td>memory-to-memory move</td>
</tr>
<tr>
<td></td>
<td>register-to-register move</td>
</tr>
<tr>
<td></td>
<td>input (from I/O device)</td>
</tr>
<tr>
<td></td>
<td>output (to I/O device)</td>
</tr>
<tr>
<td></td>
<td>push, pop (to/from stack)</td>
</tr>
<tr>
<td>Arithmetic</td>
<td>integer (binary + decimal) or FP</td>
</tr>
<tr>
<td></td>
<td>Add, Subtract, Multiply, Divide</td>
</tr>
<tr>
<td>Shift</td>
<td>shift left/right, rotate left/right</td>
</tr>
<tr>
<td>Logical</td>
<td>not, and, or, set, clear</td>
</tr>
<tr>
<td>Control (Jump/Branch)</td>
<td>unconditional, conditional</td>
</tr>
<tr>
<td>Subroutine Linkage</td>
<td>call, return</td>
</tr>
<tr>
<td>Interrupt</td>
<td>trap, return</td>
</tr>
<tr>
<td>Synchronization</td>
<td>test &amp; set (atomic r-m-w)</td>
</tr>
<tr>
<td>String</td>
<td>search, translate</td>
</tr>
<tr>
<td>Graphics (MMX)</td>
<td>parallel subword ops (4 16bit add)</td>
</tr>
</tbody>
</table>
## Top 10 80x86 Instructions

<table>
<thead>
<tr>
<th>Rank</th>
<th>Instruction</th>
<th>Integer</th>
<th>Average</th>
<th>Percent total executed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>load</td>
<td></td>
<td></td>
<td>22%</td>
</tr>
<tr>
<td>2</td>
<td>conditional branch</td>
<td></td>
<td></td>
<td>20%</td>
</tr>
<tr>
<td>3</td>
<td>compare</td>
<td></td>
<td></td>
<td>16%</td>
</tr>
<tr>
<td>4</td>
<td>store</td>
<td></td>
<td></td>
<td>12%</td>
</tr>
<tr>
<td>5</td>
<td>add</td>
<td></td>
<td></td>
<td>8%</td>
</tr>
<tr>
<td>6</td>
<td>and</td>
<td></td>
<td></td>
<td>6%</td>
</tr>
<tr>
<td>7</td>
<td>sub</td>
<td></td>
<td></td>
<td>5%</td>
</tr>
<tr>
<td>8</td>
<td>move register-register</td>
<td></td>
<td></td>
<td>4%</td>
</tr>
<tr>
<td>9</td>
<td>call</td>
<td></td>
<td></td>
<td>1%</td>
</tr>
<tr>
<td>10</td>
<td>return</td>
<td></td>
<td></td>
<td>1%</td>
</tr>
</tbody>
</table>

Total 96%

- Simple instructions dominate instruction frequency
Operation Summary

- Support these simple instructions, since they will dominate the number of instructions executed:

  load, store, add, subtract, move register-register, and, shift, compare equal, compare not equal, branch, jump, call, return;
Compilers and Instruction Set Architectures

• Ease of compilation
  ° orthogonality: no special registers, few special cases, all operand modes available with any data type or instruction type
  ° completeness: support for a wide range of operations and target applications
  ° regularity: no overloading for the meanings of instruction fields
  ° streamlined: resource needs easily determined

• Register Assignment is critical too
  ° Easier if lots of registers
Summary of Compiler Considerations

• Provide at least 16 general purpose registers plus separate floating-point registers,

• Be sure all addressing modes apply to all data transfer instructions,

• Aim for a minimalist instruction set.
MIPS I Operation Overview

- Arithmetic logical
  - Add, AddU, Sub, SubU, And, Or, Xor, Nor, SLT, SLTU
  - AddI, AddIU, SLTI, SLTIU, AndI, OrI, XorI, LUI
  - SLL, SRL, SRA, SLLV, SRLV, SRAV

- Memory Access
  - LB, LBU, LH, LHU, LW, LWL, LWR
  - SB, SH, SW, SWL, SWR
Multiply / Divide

- Start multiply, divide
  - MULT rs, rt
  - MULTU rs, rt
  - DIV rs, rt
  - DIVU rs, rt
- Move result from multiply, divide
  - MFHI rd
  - MFLO rd
- Move to HI or LO
  - MTHI rd
  - MTLO rd

- Why not Third field for destination?
  (Hint: how many clock cycles for multiply or divide vs. add?)
Data Types

Bit: 0, 1

Bit String: sequence of bits of a particular length
- 4 bits is a nibble
- 8 bits is a byte
- 16 bits is a half-word
- 32 bits is a word
- 64 bits is a double-word

Character:
- ASCII 7 bit code

Decimal:
- digits 0-9 encoded as 0000b thru 1001b
- two decimal digits packed per 8 bit byte

Integers:
- 2's Complement

Floating Point:
- Single Precision
- Double Precision
- Extended Precision

How many +/- #'s?
Where is decimal pt?
How are +/- exponents represented?
Operand Size Usage

- Doubleword: 0% (Int Avg.), 69% (FP Avg.)
- Word: 19% (Int Avg.), 74% (FP Avg.)
- Halfword: 0% (Int Avg.), 31% (FP Avg.)
- Byte: 0% (Int Avg.), 7% (FP Avg.)

Frequency of reference by size

- Support these data sizes and types:
  - 8-bit, 16-bit, 32-bit integers and 32-bit and 64-bit IEEE 754 floating point numbers
### MIPS arithmetic instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Example</th>
<th>Meaning</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>add</td>
<td>add $1,$2,$3</td>
<td>$1 = $2 + $3</td>
<td>3 operands; exception possible</td>
</tr>
<tr>
<td>subtract</td>
<td>sub $1,$2,$3</td>
<td>$1 = $2 – $3</td>
<td>3 operands; exception possible</td>
</tr>
<tr>
<td>add immediate</td>
<td>addi $1,$2,100</td>
<td>$1 = $2 + 100</td>
<td>+ constant; exception possible</td>
</tr>
<tr>
<td>add unsigned</td>
<td>addu $1,$2,$3</td>
<td>$1 = $2 + $3</td>
<td>3 operands; no exceptions</td>
</tr>
<tr>
<td>subtract unsigned</td>
<td>subu $1,$2,$3</td>
<td>$1 = $2 – $3</td>
<td>3 operands; no exceptions</td>
</tr>
<tr>
<td>add imm. unsigned</td>
<td>addiu $1,$2,100</td>
<td>$1 = $2 + 100</td>
<td>+ constant; no exceptions</td>
</tr>
<tr>
<td>multiply</td>
<td>mult $2,$3</td>
<td>Hi, Lo = $2 x $3</td>
<td>64-bit signed product</td>
</tr>
<tr>
<td>multiply unsigned</td>
<td>multu$2,$3</td>
<td>Hi, Lo = $2 x $3</td>
<td>64-bit unsigned product</td>
</tr>
<tr>
<td>divide</td>
<td>div $2,$3</td>
<td>Lo = $2 ÷ $3, Hi = $2 mod $3</td>
<td>Lo = quotient, Hi = remainder</td>
</tr>
<tr>
<td>divide unsigned</td>
<td>divu $2,$3</td>
<td>Lo = $2 ÷ $3, Hi = $2 mod $3</td>
<td>Unsigned quotient &amp; remainder</td>
</tr>
<tr>
<td>Move from Hi</td>
<td>mfhi $1</td>
<td>$1 = Hi</td>
<td>Used to get copy of Hi</td>
</tr>
<tr>
<td>Move from Lo</td>
<td>mflo $1</td>
<td>$1 = Lo</td>
<td>Used to get copy of Lo</td>
</tr>
</tbody>
</table>

**Which add for address arithmetic? Which add for integers?**
# MIPS logical instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Example</th>
<th>Meaning</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>and</td>
<td>and $1,$2,$3</td>
<td>$1 = $2 &amp; $3</td>
<td>3 reg. operands; Logical AND</td>
</tr>
<tr>
<td>or</td>
<td>or $1,$2,$3</td>
<td>$1 = $2</td>
<td>$3</td>
</tr>
<tr>
<td>xor</td>
<td>xor $1,$2,$3</td>
<td>$1 = $2 ⊕ $3</td>
<td>3 reg. operands; Logical XOR</td>
</tr>
<tr>
<td>nor</td>
<td>nor $1,$2,$3</td>
<td>$1 = \sim($2</td>
<td>$3)</td>
</tr>
<tr>
<td>and immediate</td>
<td>andi $1,$2,10</td>
<td>$1 = $2 &amp; 10</td>
<td>Logical AND reg, constant</td>
</tr>
<tr>
<td>or immediate</td>
<td>ori $1,$2,10</td>
<td>$1 = $2</td>
<td>10</td>
</tr>
<tr>
<td>xor immediate</td>
<td>xori $1,$2,10</td>
<td>$1 = \sim$2 &amp;~10</td>
<td>Logical XOR reg, constant</td>
</tr>
<tr>
<td>shift left logical</td>
<td>sll $1,$2,10</td>
<td>$1 = $2 &lt;&lt; 10</td>
<td>Shift left by constant</td>
</tr>
<tr>
<td>shift right logical</td>
<td>srl $1,$2,10</td>
<td>$1 = $2 &gt;&gt; 10</td>
<td>Shift right by constant</td>
</tr>
<tr>
<td>shift right arithm.</td>
<td>sra $1,$2,10</td>
<td>$1 = $2 &gt;&gt; 10</td>
<td>Shift right (sign extend)</td>
</tr>
<tr>
<td>shift left logical</td>
<td>slv $1,$2,$3</td>
<td>$1 = $2 &lt;&lt; $3</td>
<td>Shift left by variable</td>
</tr>
<tr>
<td>shift right logical</td>
<td>srlv $1,$2,3</td>
<td>$1 = $2 &gt;&gt; $3</td>
<td>Shift right by variable</td>
</tr>
<tr>
<td>shift right arithm.</td>
<td>srav $1,$2,3</td>
<td>$1 = $2 &gt;&gt; $3</td>
<td>Shift right arith. by variable</td>
</tr>
</tbody>
</table>
## MIPS data transfer instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW 500(R4), R3</td>
<td>Store word</td>
</tr>
<tr>
<td>SH 502(R2), R3</td>
<td>Store half</td>
</tr>
<tr>
<td>SB 41(R3), R2</td>
<td>Store byte</td>
</tr>
<tr>
<td>LW R1, 30(R2)</td>
<td>Load word</td>
</tr>
<tr>
<td>LH R1, 40(R3)</td>
<td>Load halfword</td>
</tr>
<tr>
<td>LHU R1, 40(R3)</td>
<td>Load halfword unsigned</td>
</tr>
<tr>
<td>LB R1, 40(R3)</td>
<td>Load byte</td>
</tr>
<tr>
<td>LBU R1, 40(R3)</td>
<td>Load byte unsigned</td>
</tr>
<tr>
<td>LUI R1, 40</td>
<td>Load Upper Immediate (16 bits shifted left by 16)</td>
</tr>
</tbody>
</table>

Why need LUI?

![LUI R5 example](image)
Methods of Testing Condition

° Condition Codes

Processor status bits are set as a side-effect of arithmetic instructions (possibly on Moves) or explicitly by compare or test instructions.

ex: add r1, r2, r3
    bz label

° Condition Register

Ex: cmp r1, r2, r3
    bgt r1, label

° Compare and Branch

Ex: bgt r1, r2, label
Condition Codes

Setting CC as side effect can reduce the # of instructions

\[
\begin{align*}
X: & \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad \ldots \\
& \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad \ldots \\
& \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad \ldots \\
& \text{SUB } r0, \#1, r0 \\
& \text{BRP } X \\
\end{align*}
\]

vs.

\[
\begin{align*}
X: & \quad \ldots \\
& \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad \ldots \\
& \quad \ldots \quad \ldots \quad \ldots \quad \ldots \quad \ldots \\
& \text{SUB } r0, \#1, r0 \\
& \text{CMP } r0, \#0 \\
& \text{BRP } X \\
\end{align*}
\]

But also has disadvantages:

--- not all instructions set the condition codes; which do and which do not often confusing!
  \textit{e.g., shift instruction sets the carry bit}

--- dependency between the instruction that sets the CC and the one that tests it: to overlap their execution, may need to separate them with an instruction that does not change the CC
Conditional Branch Distance

- Distance from branch in instructions $2i \Rightarrow \leq \pm 2^{i-1} \& > 2^{i-2}$
- 25% of integer branches are $> 2$ to $\leq 4$ or -2 to -4 instructions
Conditional Branch Addressing

- PC-relative since most branches are relatively close to the current PC address
- At least 8 bits suggested (± 128 instructions)
- Compare Equal/Not Equal most important for integer programs (86%)

<table>
<thead>
<tr>
<th>Comparison Type</th>
<th>Int Avg.</th>
<th>FP Avg.</th>
</tr>
</thead>
<tbody>
<tr>
<td>EQ/NE</td>
<td>86%</td>
<td>7%</td>
</tr>
<tr>
<td>LT/GE</td>
<td>7%</td>
<td>40%</td>
</tr>
<tr>
<td>GT/LE</td>
<td>7%</td>
<td>23%</td>
</tr>
<tr>
<td>LT/GE</td>
<td>37%</td>
<td></td>
</tr>
</tbody>
</table>

Frequency of comparison types in branches
MIPS Compare and Branch

° Compare and Branch
  • BEQ rs, rt, offset if R[rs] == R[rt] then PC-relative branch
  • BNE rs, rt, offset <>

° Compare to zero and Branch
  • BLEZ rs, offset if R[rs] <= 0 then PC-relative branch
  • BGTZ rs, offset >
  • BLT <
  • BGEZ >=
  • BLTZAL rs, offset if R[rs] < 0 then branch and link (into R 31)
  • BGEZAL >=

° Remaining set of compare and branch take two instructions

° Almost all comparisons are against zero!
# MIPS jump, branch, compare instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Example</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>branch on equal</td>
<td>beq $1,$2,100</td>
<td>if ($1 == $2) go to PC+4+100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Equal test; PC relative branch</td>
</tr>
<tr>
<td>branch on not eq.</td>
<td>bne $1,$2,100</td>
<td>if ($1!= $2) go to PC+4+100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Not equal test; PC relative</td>
</tr>
<tr>
<td>set on less than</td>
<td>slt $1,$2,$3</td>
<td>if ($2 &lt; $3) $1=1; else $1=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Compare less than; 2’s comp.</td>
</tr>
<tr>
<td>set less than imm.</td>
<td>slti $1,$2,100</td>
<td>if ($2 &lt; 100) $1=1; else $1=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Compare &lt; constant; 2’s comp.</td>
</tr>
<tr>
<td>set less than uns.</td>
<td>sltu $1,$2,$3</td>
<td>if ($2 &lt; $3) $1=1; else $1=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Compare less than; natural numbers</td>
</tr>
<tr>
<td>set l. t. imm. uns.</td>
<td>sltiu $1,$2,100</td>
<td>if ($2 &lt; 100) $1=1; else $1=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Compare &lt; constant; natural numbers</td>
</tr>
<tr>
<td>jump</td>
<td>j 10000</td>
<td>go to 10000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Jump to target address</td>
</tr>
<tr>
<td>jump register</td>
<td>jr $31</td>
<td>go to $31</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For switch, procedure return</td>
</tr>
<tr>
<td>jump and link</td>
<td>jal 10000</td>
<td>$31 = PC + 4; go to 10000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For procedure call</td>
</tr>
</tbody>
</table>
Signed vs. Unsigned Comparison

R1 = 0...00 0000 0000 0000 0000 0001  two
R2 = 0...00 0000 0000 0000 0010  two
R3 = 1...11 1111 1111 1111 1111  two

After executing these instructions:

- slt  r4, r2, r1 ; if (r2 < r1) r4 = 1; else r4 = 0
- slt  r5, r3, r1 ; if (r3 < r1) r5 = 1; else r5 = 0
- sltu r6, r2, r1 ; if (r2 < r1) r6 = 1; else r6 = 0
- sltu r7, r3, r1 ; if (r3 < r1) r7 = 1; else r7 = 0

What are values of registers r4 - r7? Why?

r4 =     ; r5 =     ; r6 =     ; r7 =     ;
Calls: Why Are Stacks So Great?

Stacking of Subroutine Calls & Returns and Environments:

Some machines provide a memory stack as part of the architecture (e.g., VAX)

Sometimes stacks are implemented via software convention (e.g., MIPS)
Memory Stacks

Useful for stacked environments/subroutine call & return even if operand stack not part of architecture

Stacks that Grow Up vs. Stacks that Grow Down:

How is empty stack represented?

Little --> Big/Last Full

POP: Read from Mem(SP)  Decrement SP
PUSH: Increment SP  Write to Mem(SP)

Little --> Big/Next Empty

POP: Decrement SP  Read from Mem(SP)
PUSH: Write to Mem(SP)  Increment SP
Call-Return Linkage: Stack Frames

- Reference args and local variables at fixed (positive) offset from FP.
- Grows and shrinks during expression evaluation.

- Many variations on stacks possible (up/down, last pushed / next).
- Block structured languages contain link to lexically enclosing frame.
- Compilers normally keep scalar variables in registers, not memory!
## MIPS: Software conventions for Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>zero constant 0</td>
</tr>
<tr>
<td>1</td>
<td>at reserved for assembler</td>
</tr>
<tr>
<td>2</td>
<td>v0 expression evaluation &amp;</td>
</tr>
<tr>
<td>3</td>
<td>v1 function results</td>
</tr>
<tr>
<td>4</td>
<td>a0 arguments</td>
</tr>
<tr>
<td>5</td>
<td>a1</td>
</tr>
<tr>
<td>6</td>
<td>a2</td>
</tr>
<tr>
<td>7</td>
<td>a3</td>
</tr>
<tr>
<td>8</td>
<td>t0 temporary: caller saves</td>
</tr>
<tr>
<td></td>
<td>(callee can clobber)</td>
</tr>
<tr>
<td>9</td>
<td>t1</td>
</tr>
<tr>
<td>10</td>
<td>t2</td>
</tr>
<tr>
<td>11</td>
<td>t3</td>
</tr>
<tr>
<td>12</td>
<td>t4</td>
</tr>
<tr>
<td>13</td>
<td>t5</td>
</tr>
<tr>
<td>14</td>
<td>t6</td>
</tr>
<tr>
<td>15</td>
<td>t7</td>
</tr>
<tr>
<td>16</td>
<td>s0 callee saves</td>
</tr>
<tr>
<td></td>
<td>... (caller can clobber)</td>
</tr>
<tr>
<td>23</td>
<td>s7</td>
</tr>
<tr>
<td>24</td>
<td>t8 temporary (cont’d)</td>
</tr>
<tr>
<td>25</td>
<td>t9</td>
</tr>
<tr>
<td>26</td>
<td>k0 reserved for OS kernel</td>
</tr>
<tr>
<td>27</td>
<td>k1</td>
</tr>
<tr>
<td>28</td>
<td>gp Pointer to global area</td>
</tr>
<tr>
<td>29</td>
<td>sp Stack pointer</td>
</tr>
<tr>
<td>30</td>
<td>fp frame pointer</td>
</tr>
<tr>
<td>31</td>
<td>ra Return Address (HW)</td>
</tr>
</tbody>
</table>

Plus a 3-deep stack of mode bits.
MIPS / GCC Calling Conventions

fact:
addiu $sp, $sp, -32
sw $ra, 20($sp)
sw $fp, 16($sp)
addiu $fp, $sp, 32
...
sw $a0, 0($fp)
...
lw $31, 20($sp)
lw $fp, 16($sp)
addiu $sp, $sp, 32
jr $31

First four arguments passed in registers.
Details of the MIPS instruction set

- Register zero **always** has the value **zero** (even if you try to write it)
- Branch/jump **and link** put the return addr. PC+4 into the link register (R31)
- All instructions change **all 32 bits** of the destination register (including lui, lb, lh) and all read all 32 bits of sources (add, sub, and, or, …)
- Immediate arithmetic and logical instructions are extended as follows:
  - logical immediates ops are zero extended to 32 bits
  - arithmetic immediates ops are sign extended to 32 bits (including addu)
- The data loaded by the instructions lb and lh are extended as follows:
  - lbu, lhu are zero extended
  - lb, lh are sign extended
- Overflow can occur in these arithmetic and logical instructions:
  - add, sub, addi
  - it cannot occur in addu, subu, addiu, and, or, xor, nor, shifts, mult, multu, div, divu
Delayed Branches

- In the “Raw” MIPS the instruction after the branch is executed even when the branch is taken?
  - This is hidden by the assembler for the MIPS “virtual machine”
  - allows the compiler to better utilize the instruction pipeline (?)
By the end of Branch instruction, the CPU knows whether or not the branch will take place.

However, it will have fetched the next instruction by then, regardless of whether or not a branch will be taken.

Why not execute it?
Filling Delayed Branches

Branch:

- Inst Fetch
- Dcd & Op Fetch
- Execute

execute successor

even if branch taken!

Then branch target
or continue

Single delay slot
impacts the critical path

- Compiler can fill a single delay slot with a useful instruction 50% of the time.
  - try to move down from above jump
  - move up from target, if safe

Is this violating the ISA abstraction?

```
add r3, r1, r2
sub r4, r4, 1
bz r4, LL
NOP

... 

LL: add rd, ...
```
Miscellaneous MIPS I instructions

- **break**  A breakpoint trap occurs, transfers control to exception handler
- **syscall** A system trap occurs, transfers control to exception handler
- **coprocessor instrs.** Support for floating point
- **TLB instructions** Support for virtual memory: discussed later
- **restore from exception** Restores previous interrupt mask & mode bits into status register
- **load word left/right** Supports misaligned word loads
- **store word left/right** Supports misaligned word stores
Performance

° **Purchasing perspective**
  - given a collection of machines, which has the
    - best performance ?
    - least cost ?
    - best performance / cost ?

° **Design perspective**
  - faced with design options, which has the
    - best performance improvement ?
    - least cost ?
    - best performance / cost ?

° **Both require**
  - basis for comparison
  - metric for evaluation

° **Our goal is to understand cost & performance implications of architectural choices**
Two notions of “performance”

<table>
<thead>
<tr>
<th>Plane</th>
<th>DC to Paris</th>
<th>Speed</th>
<th>Passengers</th>
<th>Throughput (pmph)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boeing 747</td>
<td>6.5 hours</td>
<td>610 mph</td>
<td>470</td>
<td>286,700</td>
</tr>
<tr>
<td>BAD/Sud Concodre</td>
<td>3 hours</td>
<td>1350 mph</td>
<td>132</td>
<td>178,200</td>
</tr>
</tbody>
</table>

Which has higher performance?

- **Time to do the task (Execution Time)**
  - execution time, response time, latency
- **Tasks per day, hour, week, sec, ns. .. (Performance)**
  - throughput, bandwidth

Response time and throughput often are in opposition
Definitions

- Performance is in units of things-per-second
  - bigger is better
- If we are primarily concerned with response time
  - performance(x) = \( \frac{1}{\text{execution\_time}(x)} \)

"X is n times faster than Y" means

\[
\frac{\text{Performance}(X)}{\text{Performance}(Y)} = n
\]
Example

- Time of Concorde vs. Boeing 747?
  - Concord is $1350 \text{ mph} / 610 \text{ mph} = 2.2$ times faster
  - $= 6.5 \text{ hours} / 3 \text{ hours}$

- Throughput of Concorde vs. Boeing 747?
  - Concord is $178,200 \text{ pmpm} / 286,700 \text{ pmpm} = 0.62$ “times faster”
  - Boeing is $286,700 \text{ pmpm} / 178,200 \text{ pmpm} = 1.6$ “times faster”

- Boeing is 1.6 times ("60%") faster in terms of throughput
- Concord is 2.2 times ("120%") faster in terms of flying time

We will focus primarily on execution time for a single job
Basis of Evaluation

<table>
<thead>
<tr>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>• representative</td>
<td>• very specific</td>
</tr>
<tr>
<td>• portable</td>
<td>• non-portable</td>
</tr>
<tr>
<td>• widely used</td>
<td>• difficult to run, or measure</td>
</tr>
<tr>
<td>• improvements</td>
<td>• hard to identify cause</td>
</tr>
<tr>
<td>useful in reality</td>
<td></td>
</tr>
<tr>
<td>• easy to run, early in</td>
<td>• less representative</td>
</tr>
<tr>
<td>design cycle</td>
<td></td>
</tr>
<tr>
<td>• identify peak</td>
<td>• easy to “fool”</td>
</tr>
<tr>
<td>capability and</td>
<td></td>
</tr>
<tr>
<td>potential bottlenecks</td>
<td></td>
</tr>
</tbody>
</table>

- Actual Target Workload
- Full Application Benchmarks
- Small “Kernel” Benchmarks
- Microbenchmarks

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SPEC95

° Eighteen application benchmarks (with inputs) reflecting a technical computing workload
° Eight integer
  • go, m88ksim, gcc, compress, li, ijpeg, perl, vortex
° Ten floating-point intensive
  • tomcatv, swim, su2cor, hydro2d, mgrid, applu, turb3d, apsi, fppp, wave5
° Must run with standard compiler flags
  • eliminate special undocumented incantations that may not even generate working code for real programs
Metrics of performance

Each metric has a place and a purpose, and each can be misused.
Aspects of CPU Performance

\[
\text{CPU time} = \frac{\text{Seconds}}{\text{Program}} = \text{Instructions} \times \frac{\text{Cycles}}{\text{Instruction}} \times \frac{\text{Seconds}}{\text{Cycle}}
\]

<table>
<thead>
<tr>
<th></th>
<th>instr. count</th>
<th>CPI</th>
<th>clock rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compiler</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Instr. Set Arch.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Organization</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CPI

“Average cycles per instruction”

\[
CPI = \frac{(CPU \ Time \times \ Clock \ Rate)}{Instruction \ Count}
= \frac{Clock \ Cycles}{Instruction \ Count}
\]

CPU time = ClockCycleTime \* \sum_{i=1}^{n} CPI_i \times I_i

CPI = \sum_{i=1}^{n} CPI_i \times F_i \quad \text{where} \quad F_i = \frac{I_i}{Instruction \ Count}

"instruction frequency"

Invest Resources where time is Spent!
Example (RISC processor)

<table>
<thead>
<tr>
<th>Op</th>
<th>Freq</th>
<th>Cycles</th>
<th>CPI(i)</th>
<th>% Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>50%</td>
<td>1</td>
<td>.5</td>
<td>23%</td>
</tr>
<tr>
<td>Load</td>
<td>20%</td>
<td>5</td>
<td>1.0</td>
<td>45%</td>
</tr>
<tr>
<td>Store</td>
<td>10%</td>
<td>3</td>
<td>.3</td>
<td>14%</td>
</tr>
<tr>
<td>Branch</td>
<td>20%</td>
<td>2</td>
<td>.4</td>
<td>18%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.2</td>
</tr>
</tbody>
</table>

Typical Mix

How much faster would the machine be is a better data cache reduced the average load time to 2 cycles?

How does this compare with using branch prediction to shave a cycle off the branch time?

What if two ALU instructions could be executed at once?
Amdahl's Law

Speedup due to enhancement E:

\[
\text{Speedup}(E) = \frac{\text{ExTime w/o E}}{\text{ExTime w/ E}} = \frac{\text{Performance w/ E}}{\text{Performance w/o E}}
\]

Suppose that enhancement E accelerates a fraction \( F \) of the task by a factor \( S \) and the remainder of the task is unaffected, then,

\[
\text{ExTime(with E)} \leq ((1-F) + F/S) \times \text{ExTime(without E)}
\]

\[
\text{Speedup(with E)} \leq \frac{1}{(1-F) + F/S}
\]
Summary: Salient features of MIPS I

- **32-bit fixed format inst** (3 formats)
- **32 32-bit GPR** (R0 contains zero) and 32 FP registers (and HI LO)
  - partitioned by software convention
- **3-address, reg-reg arithmetic instr.**
- **Single address mode for load/store:** base+displacement
  - no indirection, scaled
  - 16-bit immediate plus LUI
- **Simple branch conditions**
  - compare against zero or two registers for =, ≠
  - no integer condition codes
- **Delayed branch**
  - execute instruction after the branch (or jump) even if the branch is taken (Compiler can fill a delayed branch with useful work about 50% of the time)
Summary: Instruction set design (MIPS)

- Use general purpose registers with a load-store architecture: **YES**
- Provide at least 16 general purpose registers plus separate floating-point registers: **31 GPR & 32 FPR**
- Support basic addressing modes: displacement (with an address offset size of 12 to 16 bits), immediate (size 8 to 16 bits), and register deferred: **YES**; 16 bits for immediate, displacement (\(\text{disp}=0 \Rightarrow \text{register deferred}\))
- All addressing modes apply to all data transfer instructions: **YES**
- Use fixed instruction encoding if interested in performance and use variable instruction encoding if interested in code size: **Fixed**
- Support these data sizes and types: 8-bit, 16-bit, 32-bit integers and 32-bit and 64-bit IEEE 754 floating point numbers: **YES**
- Support these simple instructions, since they will dominate the number of instructions executed: load, store, add, subtract, move register-register, and, shift, compare equal, compare not equal, branch (with a PC-relative address at least 8-bits long), jump, call, and return: **YES, 16b**
- Aim for a minimalist instruction set: **YES**
Summary: Evaluating Instruction Sets?

Design-time metrics:
° Can it be implemented, in how long, at what cost?
° Can it be programmed? Ease of compilation?

Static Metrics:
° How many bytes does the program occupy in memory?

Dynamic Metrics:
° How many instructions are executed?
° How many bytes does the processor fetch to execute the program?
° How many clocks are required per instruction?
° How "lean" a clock is practical?

**Best Metric:** Time to execute the program!

NOTE: this depends on instructions set, processor organization, and compilation techniques.