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Features

♦ Soft Decision Decoder
♦ Trace-back method for survivor memory
♦ The following parameters can be configured to meet your needs:
  – Soft decision word length
  – Constraint length (K)
  – Data speed (by changing the number of ACS cells)
  – The length of the trace-back
  – Coding rate (R), also punctured coding rates available
  – Coding polyynom

Applications

Wireless telecommunication
♦ Digital cellular phones
♦ Wireless lans
♦ Satellites, satellite ground stations

Consumer electronics
♦ CD players
♦ HDTVs
♦ Set-Top-Boxes

Table 1: Core Implementation Table

<table>
<thead>
<tr>
<th>FPGA</th>
<th>CLBs</th>
<th>Global IOBs</th>
<th>IOBs¹</th>
<th>Performance (MHz)</th>
<th>Speed Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex</td>
<td>241</td>
<td>1</td>
<td>9</td>
<td>60</td>
<td>-6</td>
</tr>
</tbody>
</table>

Notes:
1. Assuming all core I/O is routed off-chip.

AllianceCore™ Facts

<table>
<thead>
<tr>
<th>Core Specifics</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Provided with Core</td>
<td>Documentation Core documentation</td>
</tr>
<tr>
<td>Design File Formats</td>
<td>.ngo, EDIF Netlist, or VHDL Source RTL</td>
</tr>
<tr>
<td>Constraints File</td>
<td>NCF</td>
</tr>
<tr>
<td>Verification Tool</td>
<td>VHDL</td>
</tr>
<tr>
<td>Schematic Symbols</td>
<td>None</td>
</tr>
<tr>
<td>Evaluation Model</td>
<td>None</td>
</tr>
<tr>
<td>Reference designs &amp; Application notes</td>
<td>None</td>
</tr>
<tr>
<td>Additional Items</td>
<td>None</td>
</tr>
</tbody>
</table>

Design Tool Requirements

| Entry/Verification Tool | VHDL RTL |

Support

Support provided by CAST, Inc.

Results below obtained with the following parameters:

| Coding rate (R) | 1/2 |
| Constraint length (K) | 7 |
| Number of soft input bits | 3 |
| Trace-back length | 55 |
| Number of ACS elements | 4 |
General Description

A Viterbi decoder performs a maximum likelihood detection of 1 bit data transmitted over a channel with inter-symbol interference (ISI). The 1-bit data to be transmitted is encoded with an n-bit convolutional code in the convolutional encoder. Figure 2 shows the simplified data path from the Convolutional Encoder to the Viterbi Decoder.

The source code version of the core allows for easy adaptation to a wide variety of applications. The Viterbi Decoder can be delivered in a specific format (see Ordering Information).
Functional Description

The Viterbi core is partitioned into modules as shown in figure 1 and described below:

**Viterbi encoder**
The encoder block encodes the data to be transmitted with defined bit rate and encoding polynomial.

**Branch metrics computation**
The BranchMetrics unit calculates the Euclidean distance between the incoming data, and the transition in Trellis. This distance is used in ACS to find the minimum path.

**Add Compare Select (ACS)**
The ACS (add-compare-select) unit calculates the path metrics to find the minimum path. The ACS unit has a RADIX-2 architecture. The number of AcsUnits is parameterizable.

**Decoder Control**
The control block controls the operation of Viterbi Decoder.

**Verification Methods**
The core model has been extensively tested using various settings of the parameters. A special encoder circuit is used as a testbench for full testing of the decoder.

**Recommended Design Experience**
The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

**Ordering Information**
The Viterbi Decoder is available for purchase directly from CAST, Inc. If the EDIF Netlist format is required, a setting for the parameters will have to be submitted before the netlist can be created. Ask CAST, Inc. for the details.

Core Modifications

The Viterbi Decoder core can easily be customized to include:
- Bit error rate (BER) monitor
- Possibility to change the modulation type between BPSK and QPSK
- Microprocessor interface can be added to allow more flexibility
- Burst and continuous data support

Please contact CAST directly for any required modifications.

PINOUT

The pinout of the Viterbi Decoder core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

### Table 2: Core Signal Pinout

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RST</td>
<td>In</td>
<td>Asynchronous reset active high</td>
</tr>
<tr>
<td>CLKD</td>
<td>In</td>
<td>Decoder clock</td>
</tr>
<tr>
<td>Q[2:0]</td>
<td>In</td>
<td>Encoding rate (1/3, 1/2, 3/4, 7/8, …)</td>
</tr>
<tr>
<td>I[n:0]</td>
<td>In</td>
<td>Decoded data input</td>
</tr>
<tr>
<td>DataValid</td>
<td>Out</td>
<td>Data ready signal</td>
</tr>
<tr>
<td>BitOut</td>
<td>Out</td>
<td>Decoded data out</td>
</tr>
</tbody>
</table>

Related Information

A.B. Carlson, Communications systems, McGraw-Hill, 1986


R. Cypher, C.B.Shung, “Generalized Trace-Back techniques for Survivor Memory Management in the

Motorola, “Convolutional Encoding and Viterbi Decoding Using the DSP56001 with a V.32 Modem Trellis Example, Motorola Inc. 1989


Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:
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   San Jose, CA 95214
   Phone: 408-559-7778
   Fax: 408-559-7114
   URL: www.xilinx.com

For general Xilinx literature, contact:
   Phone: 800-231-3386 (inside the US)
         408-879-5017 (outside the US)
   E-mail: literature@xilinx.com

For AllianceCore specific information, contact:
   Phone: 408-879-5381
   E-mail: alliancecore@xilinx.com

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