Strong ARM

Philip Chong
Strong ARM (Description)

• SA-1100, 32-bit, 5-stage pipelined RISC.
• 0.35um, 3 metal layers, at 220MHz, 2.5M transistors, 60mm^2 die, 550mW at max freq.
• JPEG: compiled C code, single-threaded.
Strong ARM (Performance)

- Blocks: 640x480 image, 24 bit full color
  - Image Splitter: 307k iters, 4.6M cycles
  - Image Blocker: 14.4k iters, 72k cycles
  - DCT: 14.4k iters, 24.5M cycles
  - Quantize: 921.6k iters, 14.8M cycles
  - Dequantize: handled by InvDCT
  - InvDCT: 14.4k iters, 22.0M cycles
  - Image Unblocker: pointers the same
  - Image Combiner: 307k iters, 3.7M cycles

- Total:
  - 69.6M+14.7M(cache misses)=84.3 cycles
  - 0.35u, 220MHz, 2.6 frames/sec, 0.38 sec/frame
  - 0.25u, 300MHz, 3.6 frames/sec, 0.28 sec/frame
Strong ARM (Power, Cost, Effort)

• Power:
  – double 550mW to get 1.1W
  – 0.42 J/frame

• Cost:
  – RAM: 5M (frame), 8M (total)
  – price: about $22
  – area: $60mm^2(uP)+280mm^2(RAM)=340mm^2$
  – $2.3e-10$ frames/(lambda^2 s)

• Effort:
  – 1-2 weeks
ARM and ASIC

Ning Zhang & Marlene Wan
**ARM+ASIC (Description)**

- implementations:
  - pure RISC processor (StrongARM)
  - DCT to configurable ASIC
  - pure ASIC (literature)
  - DSP (literature)
RISC

- Performance: 1.12 sec/frame
- Power: 0.62 J/frame
- Cost: $39
- Effort: 1.5 weeks
RISC+ASIC(DCT)

- Performance: 0.7 sec/frame
- Power: 0.3 J/frame
- Cost: ?
- Effort: 2 weeks - 1 month
ASIC (JAGUAR)

- Performance: 10msec/frame
- Power: 0.63mJ/frame
- Cost: 1.5mmx1.7mm in 0.25u
- Effort: 9-28 man-months
DSP (two TIC30’s)

- Performance: 2.75s/frame
- Power: ~1W
- Cost: $247.95
- Effort: 1 day compilation
DSP (TMS320C40)

- Performance: 2.6 s/frame
- Power: 3.2 J/frame
- Cost: $160
- Effort: 1 day compilation
ASIC

David Chinnery, Rhett Davis
ASIC (Description)

• 3 stage pipeline:
  – 2 1-D DCT:
    • 16 add/sub
    • 22 mult
    • 14 add/mult
  – Quantization

• invDCT use the same pipeline

• claim:
  – Power estimates are accurate to within about a factor of two
  – speed and area estimates are accurate to within about 20%.
ASIC (Performance)

• Assumptions:
  – 0.25 um technology provided by ST
  – 25 MHz clock rate
  – 1.0 V supply voltage
  – Custom multipliers and triple-ported register files
  – Standard cells for the rest (using a library provided by ST)

• Blocks:
  – Mpy: 960ns
  – 1-D DCT: 9600ns

• Total: 0.046s
ASIC (Power, Cost)

- **Power:**
  - Gated clocks (adds to design time)
  - Supply voltage: 1.0 V
  - Power: 483uW
  - Energy/Frame: 22.2 uJ
  - Minimal static power (100 transistors tied to clock line): 5.3 uW

- **Cost:**
  - Total chip area: 24.9mm^2
ASIC (Effort)

• Blocks:
  • Specification (3 people, 1 month)
  • Multiplier design (1 person, 3 months)
  • Register file design (1 person, 3 months)
  • Logic/VHDL design (1 person, 1 month)
  • gated clocking system design (1 person, 2 months)
  • component assembly and verification (3 people, 1 month)

• Total: 3 people, ~5 months
DSP (Description)

- TI’s TMS320C54xx DSP chip
- 16 bit fixed point, .45 mW, or at 120 mW at 200 MIPS
- high-end VC5420:
  - two parallel 100 MIPS DSP cores at 1.8V
- hardware:
  - Three 16-bit data buses and one 16-bit program memory bus
  - 40 bit ACC with 40 bit barrel shifter and two independant accumulators
  - A single cycle non-pipelined MAC
  - Single-instruction repeat and block-repeat operations for program code
  - Block-memory-move instructions for better program and data management
  - Arithmetic instructions with parallel store and parallel load
  - Up to 168K single access RAM Up to 32K dual access RAM
  - Up to 8M word external memory access
  - Six channel DMA controller
DSP (Performance)

- Computation:
  - DCT: 46.1 ms
  - Quantization: 9.22 ms
  - Encoding: 17.8 ms
  - Decoding: 21.6 ms
  - De-quantization: 9.22 ms
  - IDCT: 46.1 ms
  - Total: 149.8 ms/frame

- I/O: 92.2 ms (same time)

- Total: 6.67 frames/sec, 150 ms/frame
DSP (Power, Cost, Effort)

- **Power:**
  - core CPU: 2.5V, 113mW
  - external pins: 3.0V, 75mW
  - IDLE2(CPU+peripherals): 2.5V, 5mW
  - IDLE3(entirely): 2.5V, 0.013mW

- **Cost:**
  - Chip: $3 ea.
  - Develop Tools: ~$3k ea.

- **Effort:** ~3 man-months
Configurable Processor

Niraj Shah
Scott Weber
CP (Description)

- Tensilica's Xtensa configurable uP
- core is a 32-bit RISC, 16 general purpose registers and DSP-like features
- C program, single-threaded
- speeds: 100-250MHz.
CP (Summary)

- Performance:
  - encode: 4 frames/sec, 0.25s /frame
  - decode: 4 frames/sec, 0.25s/frame
- Energy:
  - encode: 31 mJ/frame
  - decode: 32 mJ/frame
  - power: 128 mW
- Cost:
  - encode: 28k bytes (code)
  - decode: 31.6k bytes (code)
  - die: 0.25u, 4.7-5.5 mm^2
- Effort: 100 man-hours
## Summary

<table>
<thead>
<tr>
<th></th>
<th>RISC (2)</th>
<th>RISC (1)</th>
<th>RISC+ ASIC (2)</th>
<th>ASIC (2)</th>
<th>ASIC (3)</th>
<th>DSP (2)</th>
<th>DSP (2)</th>
<th>DSP (4)</th>
<th>CP (5)</th>
</tr>
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<tbody>
<tr>
<td>Perf</td>
<td>1.12s</td>
<td>0.28s</td>
<td>0.7s</td>
<td>10ms</td>
<td>46ms</td>
<td>2.8s</td>
<td>2.6s</td>
<td>150ms</td>
<td>250ms</td>
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<tr>
<td>Power</td>
<td>0.62J</td>
<td>0.42J</td>
<td>0.3J</td>
<td>0.63mJ</td>
<td>22.2uJ</td>
<td>1W</td>
<td>3.2J</td>
<td>113mW</td>
<td>128mW</td>
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<tr>
<td>Cost</td>
<td>$39</td>
<td>340 mm^2</td>
<td>?</td>
<td>1.5x1.7 mm^2</td>
<td>24.9 mm^2</td>
<td>$248</td>
<td>$160</td>
<td>$3</td>
<td>4.7-5.5 mm^2</td>
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<tr>
<td>Effort</td>
<td>1.5 weeks</td>
<td>1-2 weeks</td>
<td>2weeks 1month</td>
<td>9-28 months</td>
<td>5months</td>
<td>1day</td>
<td>1day</td>
<td>3months</td>
<td>100 hours</td>
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</tbody>
</table>

- **Perf**: Performance metrics. Times are in seconds. RISC & RISC+ both have lower times than ASIC & DSP options.
- **Power**: Power consumption metrics. RISC & RISC+ options use less power than ASIC & DSP options. RISC+ is the least power-efficient, followed by ASIC & DSP options.
- **Cost**: Cost metrics. RISC & RISC+ are the least expensive, followed by ASIC & DSP options. RISC+ is the most expensive of the RISC options.
- **Effort**: Effort metrics. RISC & RISC+ require less effort than ASIC & DSP options. RISC+ is the most time-consuming of the RISC options.
## Summary

<table>
<thead>
<tr>
<th></th>
<th>ASIC</th>
<th>ASIC</th>
<th>DSP</th>
<th>CP</th>
<th>RISC</th>
<th>RISC+ASIC</th>
<th>RISC</th>
<th>DSP</th>
<th>DSP</th>
</tr>
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<tbody>
<tr>
<td>ms/frame</td>
<td>10</td>
<td>46</td>
<td>150</td>
<td>250</td>
<td>280</td>
<td>700</td>
<td>1,120</td>
<td>2,800</td>
<td>2,600</td>
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<tr>
<td>mJ/frame</td>
<td>0.63</td>
<td>0.22</td>
<td>28.50</td>
<td>63</td>
<td>420.00</td>
<td>300.00</td>
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<td>3,200.00</td>
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<td>m(s*j)/frame</td>
<td>0.006</td>
<td>0.010</td>
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<td>15.8</td>
<td>118</td>
<td>210</td>
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<td>18,667</td>
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<td>1,320,635</td>
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