Integration Architecture Overview
Overview

- Introduction
- Architecture Overview
- Implementation
- Example
- Summary
SOC Applications and Data Flow

**APPLICATION AREA**
- DIGITAL CAMERA
- COLOR PRINTERS
- NEXT GENERATION STB
- NETWORK SWITCHING
- SOHO MULTIMEDIA
- XDSL INTERFACE
- DIGITAL TELEVISION
- DIGITAL VIDEO SERVER
- WORLD PHONE

**SOC Data Flow**
- DMA
- CPU
- DSP
- A
- C
- MEM
- I
- O
- O

SONICS, INC.
Characteristics:

- Wide performance range
- Increasing real-time multimedia/networking traffic
- Shared memory requirements
- Complex interactions

Challenging Design
Conventional Approach

SOC Design Requirements
- New design for each system
- Match system design cycle
- Hit cost/performance goals

Design Time

System | SOC
--- | ---
| |
Overview

- Introduction
- Architecture Overview
- Implementation
- Example
- Summary
Sonics Integration Architecture

Conventional

System Bus

Peripheral Bus

Custom Interfaces

Sonics Module Interface

Allows unification of *all* on-chip communication
Integration Architecture Aspects*

- Tunable Communications Subsystems
  - Silicon Backplane™
  - Logic Backplane™
- Configurable IP Core Interface
  - Sonics Module Interface
- Design Software
  - Backplane Compiler

* Patent Pending
Bus Bandwidth Requirements

- Must satisfy sum of sustained BW
- Total bus BW > peak BW of any IP Core

Bandwidth mismatch between Bus and IP Cores

Need de-coupled Bus performance

SOC Data Flow

- DMA < 10 Mbits/sec
- CPU < 100 Mbits/sec
- DSP > 100 Mbits/sec
Computer Bus Approach

IP Core

Data

Transmit FIFO

Arbiter

Address

Receive FIFO

Computer Bus

Time
Communication Bus Approach

Transmit FIFO

Receive FIFO

IP Core

Data

IP Core

Communications Bus

Time

IP Core

TDMA

TDMA
Integration Architecture Features

From Computing
- Address-based Selection
- Write and Read Transfers
- Pipelining

From Communications
- Efficient BW De-coupling
- Guaranteed BW & Latency
- Side-band Signaling

Integration Architecture
Guaranteed Bandwidth Arbitration

- Independent arbitration for every cycle
- Two phases
  - Distributed TDMA
  - Round robin

Gives SOC designer fine control over system bandwidth
Guaranteed Latency

- Fixed latency between command/address and data/response phases
- Matches pipelined CPU model
  - High performance access to on-chip resources
- Allows routing of pipelined data through Backplane
- Latency is re-programmable in software
- Variable-latency IP Cores do not tie up the Backplane
Memory-Mapped Address Space

- IP Cores accessed *only* via Read / Write commands
- Interface Modules decode addresses for IP Core selection
- Interface Module address match logic features:
  - Variable match width
  - Multiple match regions
  - Positive / Negative decoding
  - Subtractive decoding
- Module Configuration Registers
  - Access re-programmable / hardwired Backplane features
  - IP Core device control registers
Dedicated Backplane wires (Flags) support:
- Bus-style Out-of-Band Signaling (Interrupts)
- Point-to-Point Communications (Flow control)
- Dynamic point-to-point (Retry mechanism)

Integral part of Integration Architecture
- Same design flow, timing, flexibility as address/data part

Retry Mechanism:

<table>
<thead>
<tr>
<th>Command</th>
<th>RD1</th>
<th></th>
<th></th>
<th>RD1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Response</td>
<td></td>
<td>RTRY</td>
<td></td>
<td>Valid</td>
</tr>
<tr>
<td>FlagNum</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flag[7]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Off-Chip Extension: Logic Backplane

CPU-Based ASSP

ASSP

PLD

Silicon Backplane

Logic Backplane
Overview

- Introduction
- Architecture Overview
- Implementation
- Example
- Summary
Target Module Block Diagram

Silicon Backplane Interface

- Address/Data Flow
- Address Decoder
- Configuration Registers
- Synchronizer (Optional)

Sonics Module Interface

- Clock
- Address / Control
- Data
# Sonics Module Interface: Basics

<table>
<thead>
<tr>
<th>Signal</th>
<th>Driver</th>
<th>Width</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>Any</td>
<td>1</td>
<td>Driven by Master, Slave, or other</td>
</tr>
<tr>
<td>Cmd</td>
<td>Master</td>
<td>≤ 3</td>
<td>Idle, Read, Write + extensions</td>
</tr>
<tr>
<td>Addr</td>
<td>Master</td>
<td>Varies</td>
<td>Req. Address; VC specs width</td>
</tr>
<tr>
<td>DataOut</td>
<td>Master</td>
<td>Varies</td>
<td>Write Data; VC specs width</td>
</tr>
<tr>
<td>ReqAccept</td>
<td>Slave</td>
<td>1</td>
<td>Slave accepts request</td>
</tr>
<tr>
<td>Resp</td>
<td>Slave</td>
<td>≤ 3</td>
<td>Response to prior request</td>
</tr>
<tr>
<td>DataIn</td>
<td>Slave</td>
<td>Varies</td>
<td>Read Data; valid based on Resp</td>
</tr>
<tr>
<td>RespAccept</td>
<td>Master</td>
<td>1</td>
<td>Master accepts response</td>
</tr>
</tbody>
</table>

**Simple Synchronous Read/Write Protocol**

with Variable Widths and Flow Control
VSIA Correspondence

VSIA On-chip Bus Model

- Virtual Component
- Transaction Protocol
- Bus Transfer Protocol
- Physical Bus

Sonics Integration Architecture

- Sonics Module Interface
- Silicon Backplane Protocol
- Physical Bus

Virtual Component Interface
Define System Specifications

Partition System

Select / Design IP Cores

Analyze Performance

Backplane Compiler

System Bandwidth & Latency Constraints

IP Core Requirements

Simulate / Integrate SOC

IP Cores

Silicon Backplane
Validation / Test

- Silicon Backplane is highly visible for test
  - All subsystems communicate through Backplane
- Test Interfaces:
  - Logic Backplane: 100’s MB/s
  - Snooping Module: Scan-based
- Each subsystem can be tested/validated stand-alone
Silicon Backplane Performance Roadmap

Soft and Firm versions should satisfy 90% of SOC applications
Overview

- Introduction
- Architecture Overview
- Implementation
- Example
- Summary
Set-top Box Application Example

Application
- DSS set-top box with Internet browsing capability

Cores
- CPU, MPEG decoder, V.34 modem, 2-D graphics, NTSC encoder, DES, SDRAM controller, Flash controller, etc.
Application Data Flow

Note: Partial Core List
# IP Core Clock Frequencies

<table>
<thead>
<tr>
<th>IP Core</th>
<th>MHz</th>
<th>IP Core</th>
<th>MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>54</td>
<td>MDM</td>
<td>27</td>
</tr>
<tr>
<td>XPT</td>
<td>27</td>
<td>GFX</td>
<td>27</td>
</tr>
<tr>
<td>MPV</td>
<td>27</td>
<td>ENC</td>
<td>27</td>
</tr>
<tr>
<td>MPA</td>
<td>27</td>
<td>UCR</td>
<td>6.75</td>
</tr>
<tr>
<td>SDC</td>
<td>81</td>
<td>DES</td>
<td>6.75</td>
</tr>
<tr>
<td>ROM</td>
<td>6.75</td>
<td>WAV</td>
<td>27</td>
</tr>
<tr>
<td>QPD</td>
<td>20</td>
<td>SCC</td>
<td>6.75</td>
</tr>
<tr>
<td>Silicon Backplane</td>
<td>54</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

64-bit Silicon Backplane @ 54 MHz ➔ 432 MB/s
TDMA Time Slot Assignment

Integration Architecture Benefits

- Simplifies Design
- Guarantees Performance
- Improves Efficiency
- Provides IP Plug-and-Play
- Adds Flexibility / Margin

Reduces Time-to-Market
Summary

- SOC Applications Combine Performance-Driven and Real-Time Traffic
- Proposed Integration Architecture Combines On-Chip, Off-Chip, and IP Core Protocols
  - Silicon Backplane and Logic Backplane Provide Configurable Bandwidth and Latency Guarantees
  - Module Interface Isolates IP Cores From SOC Application Requirements
  - Backplane Compiler Provides Simple User Interface
- Set-top Box SOC Example Demonstrates Advantages of the Architecture