System-on-a-Chip and Interfaces

Richard Newton
University of California at Berkeley
Framework in Which to Understand System on a Chip
IMPACT OF SUBSTITUTION
Modems shipped to North America

Unit price, $

9,600 bps or less

Source: Dataquest; McKinsey analysis
IMPACT OF SUBSTITUTION
Modems shipped to North America

Source: Dataquest; McKinsey analysis
IMPACT OF SUBSTITUTION
Modems shipped to North America

Unit price, $

28,800 and 33,600 bps

19,200 bps

9,600 bps or less

Source: Dataquest; McKinsey analysis
IMPACT OF SUBSTITUTION
Modems shipped to North America

Unit price, $

- 19,200 bps
- 28,800 and 33,600 bps
- 9,600 bps or less
- 56 Kbps

Source: Dataquest; McKinsey analysis
IMPACT OF SUBSTITUTION
Modems shipped to North America

Source: Dataquest; McKinsey analysis
WORLDWIDE SEMICONDUCTOR REVENUES GROWING RAPIDLY
Merchant semiconductor sales, $ Billions

Source: ICE, Dataquest
PC INDUSTRY LARGE DRIVER OF GROWTH FROM 1985-1995

$ Billions

- PCs: 27.1
- Non-PC computing: 46.1
- Consumer: 22.3
- Communications: 21.1
- Industrial/transportation: 14.1
- Military/civil aerospace: 0.4

CAGR: 34% 14% 21% 14% 14% 1%

Source: Dataquest; ICE status
PCs AND COMMUNICATIONS EXPECTED TO DRIVE GROWTH THROUGH 2001

$ Billions

Source: Dataquest (October 1997)
WINNERS HAVE PROFITED HANDSOMELY
Financial performance of leading players

<table>
<thead>
<tr>
<th>Segment</th>
<th>Company</th>
<th>Average operating margins, 1992-96</th>
<th>Average ROIC, 1992-96 Percent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory (mostly DRAM)</td>
<td>Micron</td>
<td>23</td>
<td>34</td>
</tr>
<tr>
<td>Microprocessors</td>
<td>Intel</td>
<td>32</td>
<td>42</td>
</tr>
<tr>
<td>Programmable logic ICs</td>
<td>Xilinx</td>
<td>27</td>
<td>42</td>
</tr>
<tr>
<td>Foundry</td>
<td>TSMC</td>
<td>32</td>
<td>25</td>
</tr>
</tbody>
</table>

Source: 10Ks; McKinsey Corporate Finance Practice; Annual reports
UNATTRACTIVE INDUSTRY RESULTS

Economic profit margin of U.S. semiconductor companies
Percent

Note: Economic profit margin is weighted (ROIC-WACC) for AMD, Analog, Cypress, IDT, Intel, LSI Logic, Micron, National, VLSI (and TI from 1995)
Source: Annual reports; Compustat
INTEL’S PROFITABILITY HAS CARRIED THE INDUSTRY
Average ROIC, 1990-97

Average WACC = 13.2

* Includes AMD, Analog Devices, Cypress, Cirrus Logic, LSI, Micron, National, VLSI, and TI
Source: Annual reports; Compustat
Background

The Seven Views of Computer Systems

Bell, Mudge & McNamara

Source: Bill Lattin, Synopsys
The Seven Views of Computer Systems

View One: Structural Levels of a Computer System
View Two: Levy’s Levels of Interpreters
View Three: Packaging Levels of Integration
View Four: A Marketplace View of Computer Classes
View Five: An Applications/Functional View of Computer Classes
View Six: The Practice of Design
View Seven: The BLAAUW Characterization of Computer Design

Source: Bill Lattin, Synopsys
View One: Hierarchy of Computer Levels

Adapted from Bell and Newell [1971]

Source: Bill Lattin, Synopsys
View Two: A Hierarchy of Interpreters

[Levy, 1974]

Source: Bill Lattin, Synopsys
View Three: Packaging Levels of Integration

This is a Structural View That Packages the Various Components (Hardware and Software) into Levels. The Levels for DEC Computers in 1978 Were as Follows:

→ 9 Applications
→ 8 Applications Components
→ 7 Special Languages
→ 6 Standard Languages
→ 5 Operating Systems
→ 4 Cabinets (to Hold Complete Hardware Systems)
→ 3 Boxes
→ 2 Modules (Printed Circuit Boards)
→ 1 Integrated Circuits

Source: Bill Lattin, Synopsys
View Four: A Marketplace View of Computer Classes

Price vs. Time for Each Machine Class

Source: Bill Lattin, Synopsys
View Five: An Applications/Functional View of Computer Classes

- **PMS Level Configuration**: A Configuration is Chosen to Match the Function to Be Performed. The User (Designer) Chooses the Amount of Primary Memory, the Number and Types of Secondary Memory, the Types of Switches, and the Number and Types of Transducers to Suit His Particular Application.

- **Physical Packaging**: Special Environmental Packaging is Used to Specialize a Computer System for Certain Environments, Such as Factory Floor, Submarine, or Aerospace Applications.

- **Data-type Emphasis**: Computers are Designed with Data-types (and Operations to Match) that are Appropriate to Their Tasks. Some Emphasize Floating-point Arithmetic, Others String Handling. Special-Purpose Processors, Such as Fast Fourier Transform Processors, Belong in This Category Also.


Source: Bill Lattin, Synopsys
Hardware Development Costs for Developing a $50K Processor in ‘74

[Phister, 1976]

Source: Bill Lattin, Synopsys
## View Seven: The Blaauw Characterization of Computer Design

### Characteristics of Design Areas

<table>
<thead>
<tr>
<th>Purpose</th>
<th>Function</th>
<th>Cost and Performance</th>
<th>Buildable and Maintainable</th>
</tr>
</thead>
<tbody>
<tr>
<td>Product</td>
<td>Principles of operation</td>
<td>Logic design</td>
<td>Release to manufacturing</td>
</tr>
<tr>
<td>Language</td>
<td>Written algorithms</td>
<td>Block diagram, expressions</td>
<td>Lists and diagrams</td>
</tr>
<tr>
<td>Quality measure</td>
<td>Consistency</td>
<td>Broad scope</td>
<td>Reliability</td>
</tr>
<tr>
<td>Meanings (used herein)</td>
<td>ISP Machine ISP</td>
<td>RT level machine; microprogrammed sequential machine (at logic level)</td>
<td>Physical realization; physical implementation</td>
</tr>
</tbody>
</table>

Source: Bill Lattin, Synopsys
The Five Views of System on a Chip

**View One:** Semiconductor Process & Packaging View

**View Two:** IP Functional View

**View Three:** IP Design Methodology View

**View Four:** System Design Methodology View

**View Five:** System Software View

Source: Bill Lattin, Synopsys
### SIA Roadmap

#### THE CHALLENGES OF CHANGING CHIPS

<table>
<thead>
<tr>
<th>Category</th>
<th>Problem</th>
<th>Key parameters</th>
<th>Trends</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Wiring levels</td>
<td>4-5 5 5-6 6 6-7 7-8</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>Chip size</td>
<td>250 mm² 300 mm² 360 mm² 430 mm² 520 mm² 620 mm²</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>Interlevel contact diameter</td>
<td>0.4 µm 0.28 µm 0.2 µm 0.14 µm 0.11 µm 0.08 µm</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>Gate dielectric thickness</td>
<td>7-12 nm 4-5 nm 4-5 nm 4-5 nm &lt;4 nm &lt;4 nm</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>to subtle, hard-to</td>
<td>350 MHz 450 MHz 600 MHz 800 MHz 1000 MHz 1100 MHz</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>variation</td>
<td>70 mV 50 mV 40 mV 30 mV 25 mV 20 mV</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>Supply voltage</td>
<td>2.5-3.3 V 1.2-2.5 V 1.2-1.8 V 1.2-1.5 V &lt;1.2 V</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
<tr>
<td></td>
<td>to be done from back of chip</td>
<td>(COB), chip-on-chip</td>
<td>1995 1998 2001 2004 2007 2010</td>
</tr>
</tbody>
</table>

Data from National Technology Roadmap for Semiconductors, 1994, Semiconductor Industry Association

Source: Bill Lattin, Synopsys
Conclusions From View One

- 20M Gates will be Here in 2000
- Multiple Power Supplies will Require DCL Descriptions (Equations vs Tables)
- Copper is Here Now (6 Layers)
- Trench DRAM Hybrid Process in 1999
- I/O Continue to Grow (Power Management EMI Analysis & Synthesis)

Source: Bill Lattin, Synopsys
View Two: IP Functional View

- Microprocessor
- Memory Sub System
- ASIC (Customer’s Logic)
- DSP
- RF (Analog)
- Mixed Signal
- I/O Systems
- On Chip Bus

Source: Bill Lattin, Synopsys
<table>
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<tr>
<th>Creation</th>
<th>Analysis</th>
<th>Integration</th>
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<tr>
<td>System</td>
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<td>System</td>
</tr>
<tr>
<td>RTL</td>
<td>RTL</td>
<td>RTL</td>
</tr>
<tr>
<td>Physical</td>
<td>Physical</td>
<td>Physical</td>
</tr>
</tbody>
</table>

Source: Bill Lattin, Synopsys
System-on-a-Chip IP Creation and Analysis Flow

Architectural Design

Digital Control
- RTL
- Logic Synthesis
- Logic Verification
- Std Cell P&R

Datapath
- Functional Description
- Logic Design & Simulation
- Performance Optimization
- Datapath Compiler
- Chip Assembly Block P&R
- DRC/LVS/Extraction Parasitic Reduction
- Full Chip Timing Verification

Memory
- Memory Behavior Model
- Decoder/Periphery Design
- Core Cell Sense Amp
- Custom Layout
- Full Chip Func Simulation

Analog
- Analog Functional Model
- Analog Circuit Design & Sim.

Source: Bill Lattin, Synopsys
System-on-a-Chip Design Flow

Architectural Design

Digital Control
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Source: Bill Lattin, Synopsys
System-on-a-Chip Integration Flow

System Abstraction
- System Physical Floorplan
- System Hardware/Software Partitioning
- System Design Planning

System Verification
- Functional
- Timing
- Power
- Physical
- Manufacturing
  - Test
  - Noise
  - Reliability
- Software

Source: Bill Lattin, Synopsys
View Four - System Design Methodology

- Problems Migrate to the IP Block Boundaries
- IP Blocks Effect Each Other
- Tools Must Enforce IP Block Boundaries
- IP Blocks Need Different Analysis Tools
  - ✔ Digital IP Blocks
  - ✔ Mixed Signal IP Blocks
  - ✔ RF IP Blocks
  - ✔ Memory IP Blocks

Source: Bill Lattin, Synopsys
SoC Model Views

Core Creation
- Core Design
- Automatic Model Creation
- Post-Design Remodeling

Core Views
- Instruction Set Architecture
- Bus Functional
- Full Function Cycle
- Timing Model
- Full-Function with Timing
- Test Model
- Floorplan/Phy Model
- Electrical Rule Model

Integration
- Functional Design
- Timing Design
- Power Design
- Physical Design
- Manufacturing Design
- Software Design

Place & Route and Chip Finishing

Source: Bill Lattin, Synopsys
Tradeoffs Among Types of System Designs

Source: Bill Lattin, Synopsys