NANOELECTRONICS AND PLASMA PROCESSING — THE NEXT 15 YEARS AND BEYOND

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OUTLINE

- The nanoelectronics revolution
- Dual frequency capacitive discharges
  - Energy and power deposition
  - Standing waves and skin effects
- The next 15 years and beyond

W.P. Allis (1901–1999)
Co-founder of the GEC

THE NANOELECTRONICS REVOLUTION

THE NANOELECTRONICS REVOLUTION

- Transistors/chip doubling every $1\frac{1}{2}$–2 years since 1959
- 1,000,000-fold decrease in cost for the same performance in the last 30 years
- In 20 years one computer will be as powerful as all those in Silicon Valley today

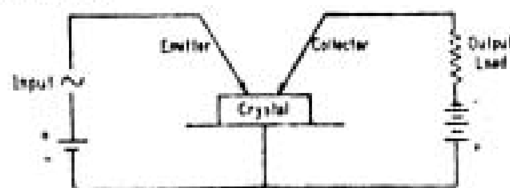
EQUIVALENT AUTOMOTIVE ADVANCE

- 60 million miles/hr
- 20 million miles/gal
- Throw away rather than pay parking fees
- 3 mm long $\times$ 1 mm wide
- Crash $3\times$ a day

THE INVENTION OF THE TRANSISTOR

The "Transistor" – an Amplifying Crystal

There was a time in the early days of radio when the "oscillating crystal" could be catalogued with sky hooks, left-handed monkey wrenches and striped paint, because no one knew how to amplify a signal with a galena, silicon or other crystal. All this is changed by the recent Bell Telephone Laboratories' announcement of the "Transistor," a small germanium-crystal unit that can amplify signals, and hence be made to oscillate.



Housed in a small metal tube less than one inch long and less than a quarter inch in diameter, the Transistor has no filament, no vacuum, and no glass envelope, and is made up only of cold solid substances. Two "catwhisker"-point contacts are made to a surface of the small germanium crystal, spaced approximately 0.002 inch apart.

The Transistor shown is connected as an amplifier in the accompanying sketch. The contact on the input side is called the "emitter" and the output contact is called the "collector" by the Bell Labs. A small positive bias of less than one volt is required on the emitter, and the output circuit consists of a negative bias of 20 to 30 volts and a suitable load. The input impedance is low (100 ohms or so), and the output impedance runs around 10,000 ohms.

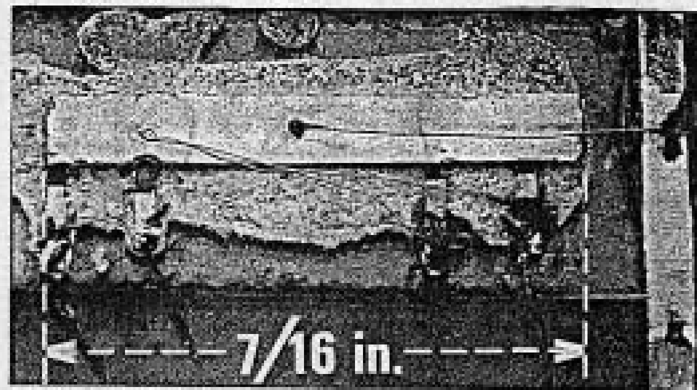
In operation, a small static current flows in both input and output circuit. A small current change in the emitter circuit causes a current change of about the same magnitude in the collector circuit. However, since the collector (output) circuit is a much higher-impedance circuit, a power gain is realized. Measuring this gain shows it to be on the order of 100, or 20 db., up through the television video range (5 Mc. or so). The present upper-frequency limit is said to be around 10 Mc., where transit-time effects limit the operation.

The Bell Labs have demonstrated complete broadcast-range superhet receivers using only Transistors for oscillator and amplifier functions (with a 1N34 second detector and selenium power rectifiers). An audio output of 25 milliwatts was obtained by using two Transistors in a push-pull connection. However, it seems likely that in the near future Transistors will find their maximum application in telephone amplifiers and large-scale computers, although their small size and zero warm-up time may make them very useful in hearing aids and other compact amplifiers.

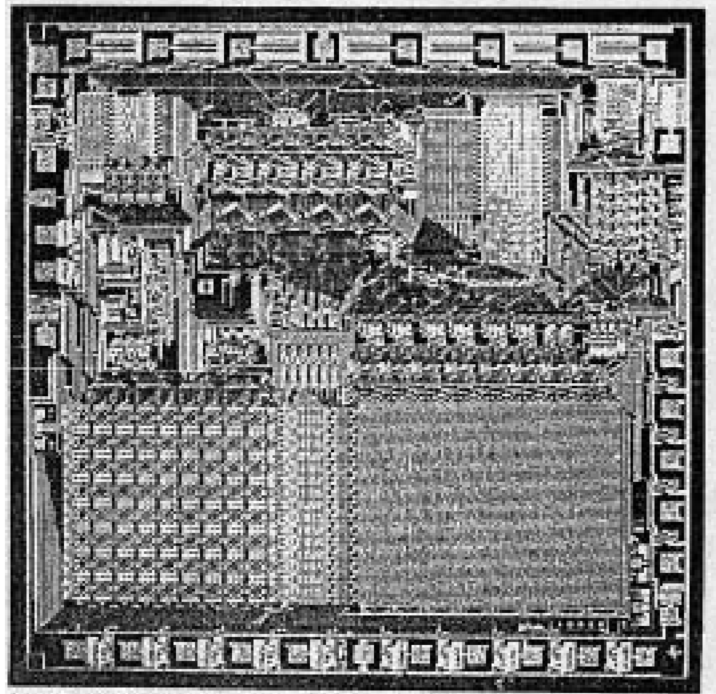
It doesn't appear that there will be much use made of Transistors in amateur work, unless it is in portable and/or compact audio amplifiers. The noise figure is said to be poor, compared to that obtainable with vacuum tubes, and this fact may limit the usefulness in some amateur applications. These clever little devices are well worth keeping an eye on. — *B. G.*

QST for October 1948

FIRST INTEGRATED CIRCUIT AND MICROPROCESSOR



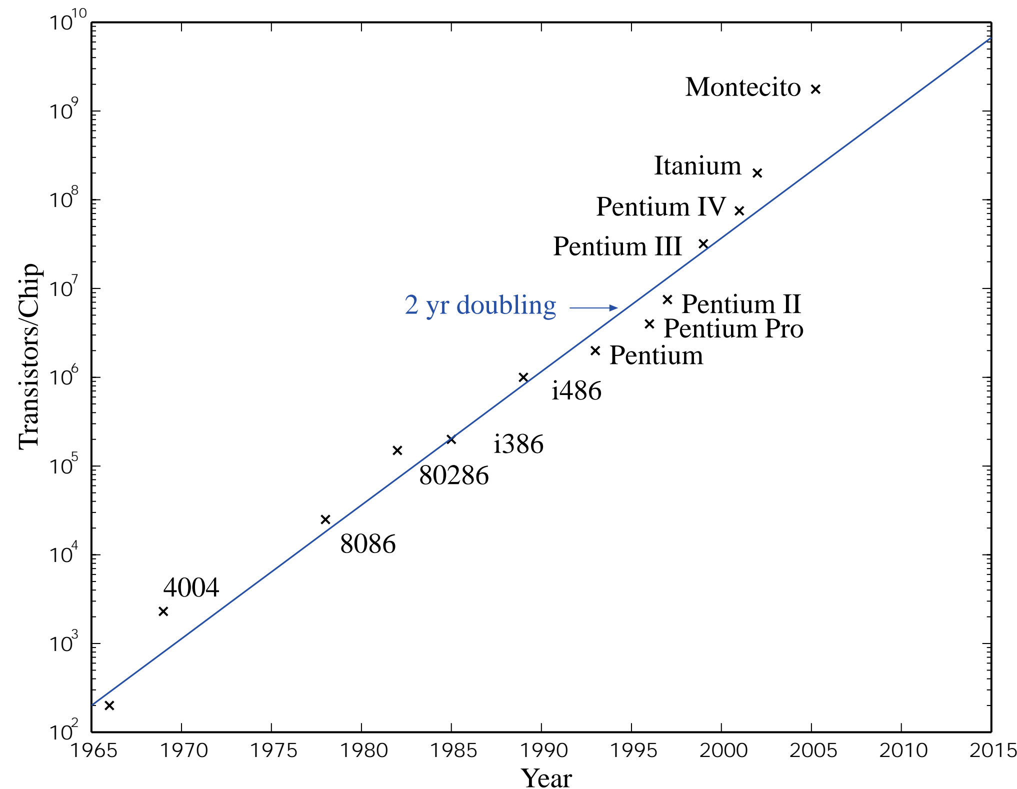
The first integrated circuit was made in 1958 by Jack Kilby of Texas Instruments.



Less than two decades later, engineers put a complete microcomputer on a chip. [Source: Texas Instruments, Inc.]

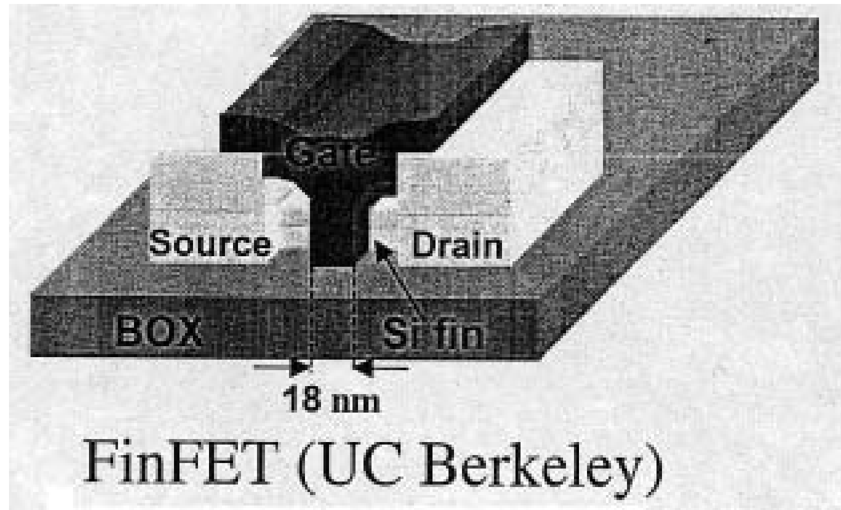
MOORE'S LAW

- "Transistors/chip double every 18 months" — Gordon Moore (1965)
  (Transistor size shrinking; chip size growing)
- Now a self-fulfilling prophecy

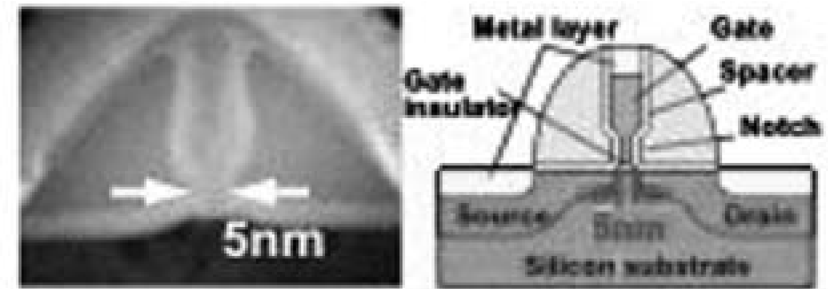


- "No exponential is forever. . . but we can delay 'forever"'
  (Gordon Moore, 2003)

DOUBLE/TRI GATE TRANSISTORS



FinFET (UC Berkeley)

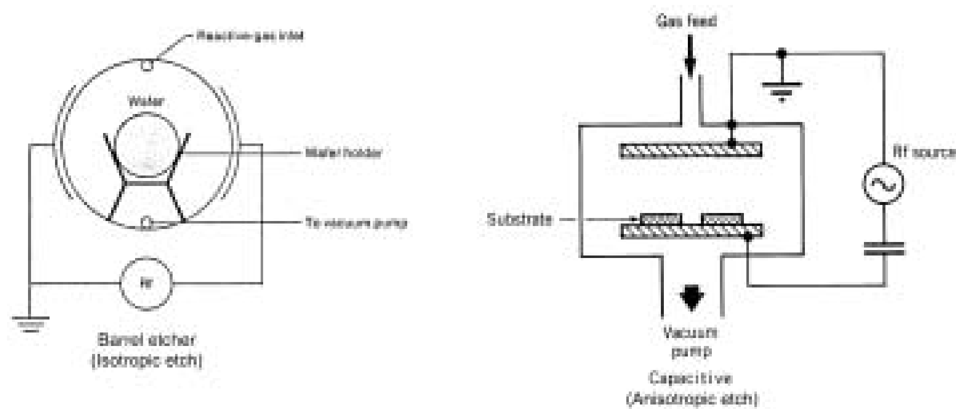


NEC 5 nm Gate

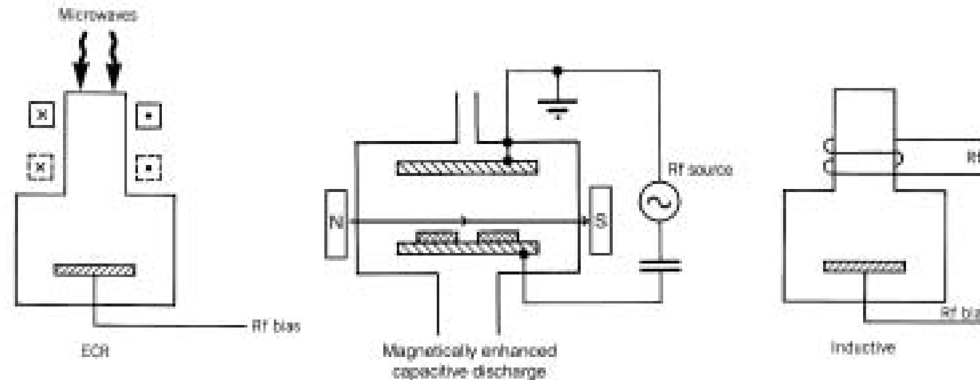
- Vertical structures can be built with current fabrication techniques
- CMOS can be scaled another 15 years
- State of the art (2005):
  - In manufacture:
    50 nm (200 atoms) gate length
    1.5 nm (5 atoms) gate oxide thickness
  - Smallest fabricated CMOS transistor (NEC):
    5 nm (20 atoms) gate length
  - Limiting gate length from simulations (desktop ic):
    4 nm (16 atoms) gate length

EVOLUTION OF ETCHING DISCHARGES

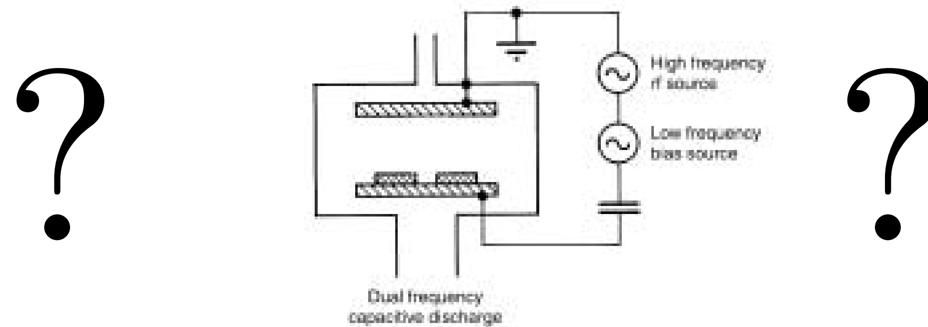
FIRST GENERATION



SECOND GENERATION



THIRD GENERATION



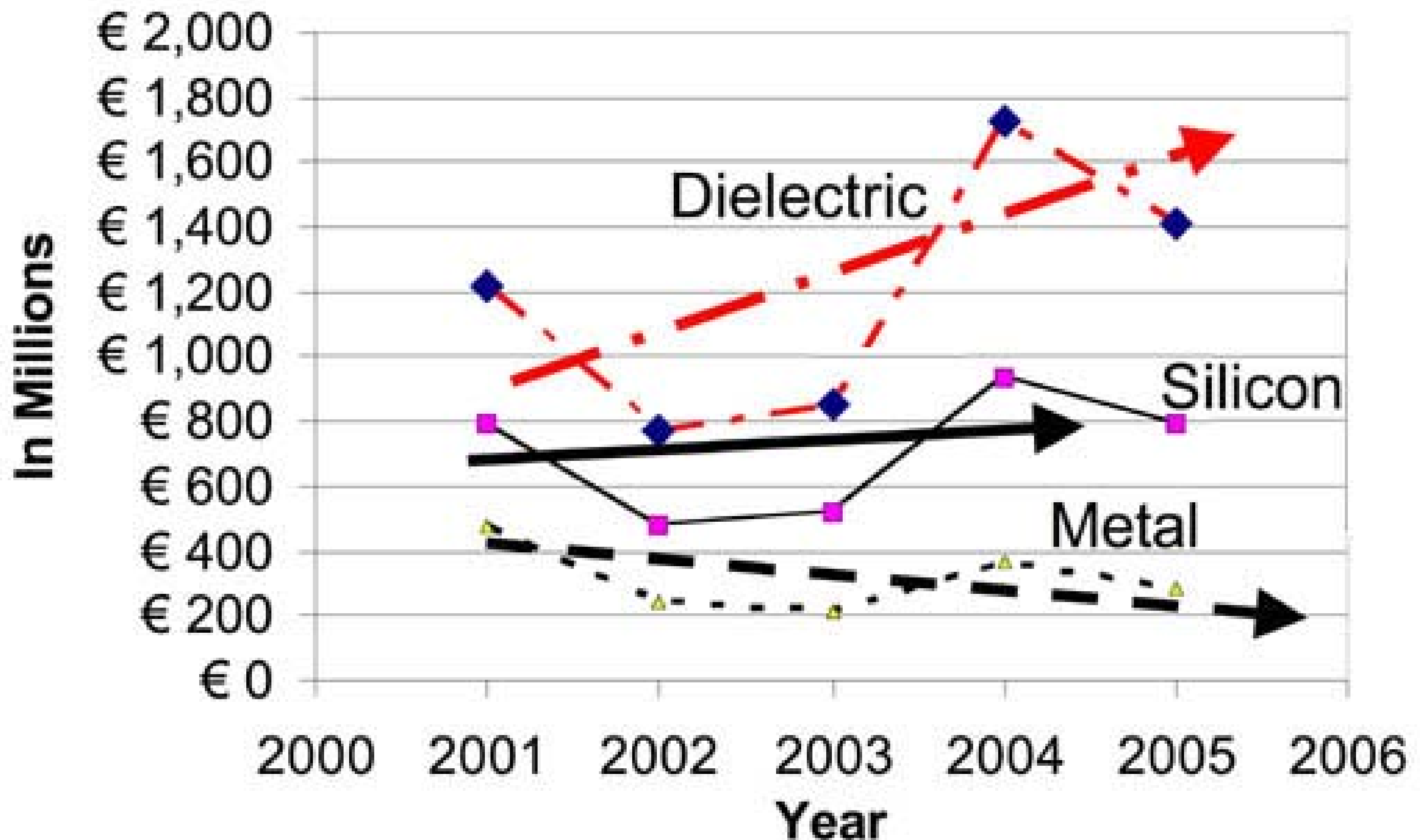
DUAL FREQUENCY CAPACITIVE DISCHARGES

WHY DUAL FREQUENCY CAPACITIVE DISCHARGES?

- Low cost
- Robust uniformity over large area
- Control of dissociation (fluorine)
- Independent control of ion flux and ion energy

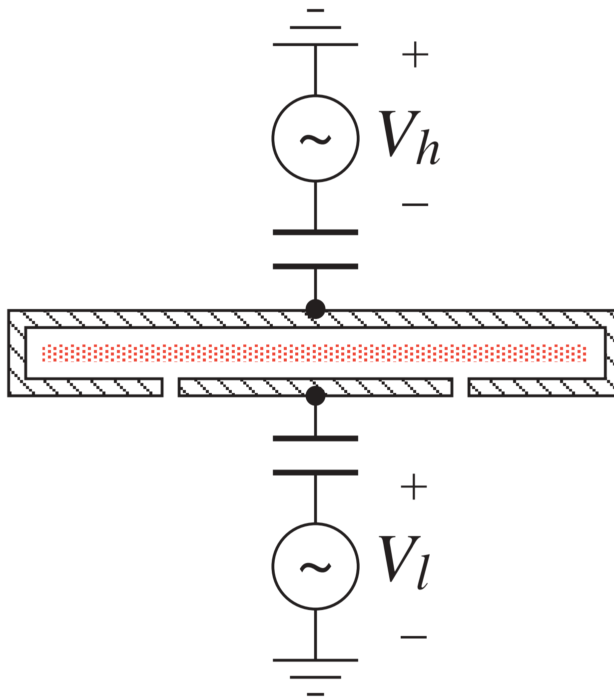
High frequency voltage controls ion flux
Low frequency voltage controls ion energy

WORLD DRY ETCH MARKET



- 54% of \$3.1B 2005 market is dielectric (dual frequency discharge)
- At 45 nm in 2008–2010, expect 16 interconnect dielectric layers

TYPICAL OPERATING CONDITIONS



- $R \sim$ 15–30 cm, $L \sim$ 1–3 cm

  $p \sim$ 30–300 mTorr, $C_4F_8/O_2/Ar$ feedstock

  High frequency $f_h \sim$ 27.1–160 MHz, $V_h \sim$ 200–500 V

  Low frequency $f_l \sim$ 2–13.56 MHz, $V_l \sim$ 500–1500 V

  Absorbed powers P_h, $P_l \sim$ 500–3000 W

CONTROL OF PLASMA DENSITY

- In a single frequency capacitive discharge

  Electron power balance $\Longrightarrow$ plasma density n

$$n \propto P_e$$

  $P_e =$ power absorbed by electrons $\propto \omega^2 V_{\rm rf}$

$$\Longrightarrow n \propto \omega^2 V_{\rm rf}$$

- For two frequencies with $\omega_h^2 V_h \gg \omega_l^2 V_l$

High frequency voltage V_h controls plasma density (ion flux)

CONTROL OF ION ENERGY

- Ion bombarding energy $\propto$ sum of low and high frequency voltages

$$\mathcal{E}_i \sim 0.41\,(V_l + V_h)$$

- Make $V_l \gg V_h$

$$\boxed{\text{Low frequency voltage } V_l \text{ controls ion energy}}$$

- Typical operating regime

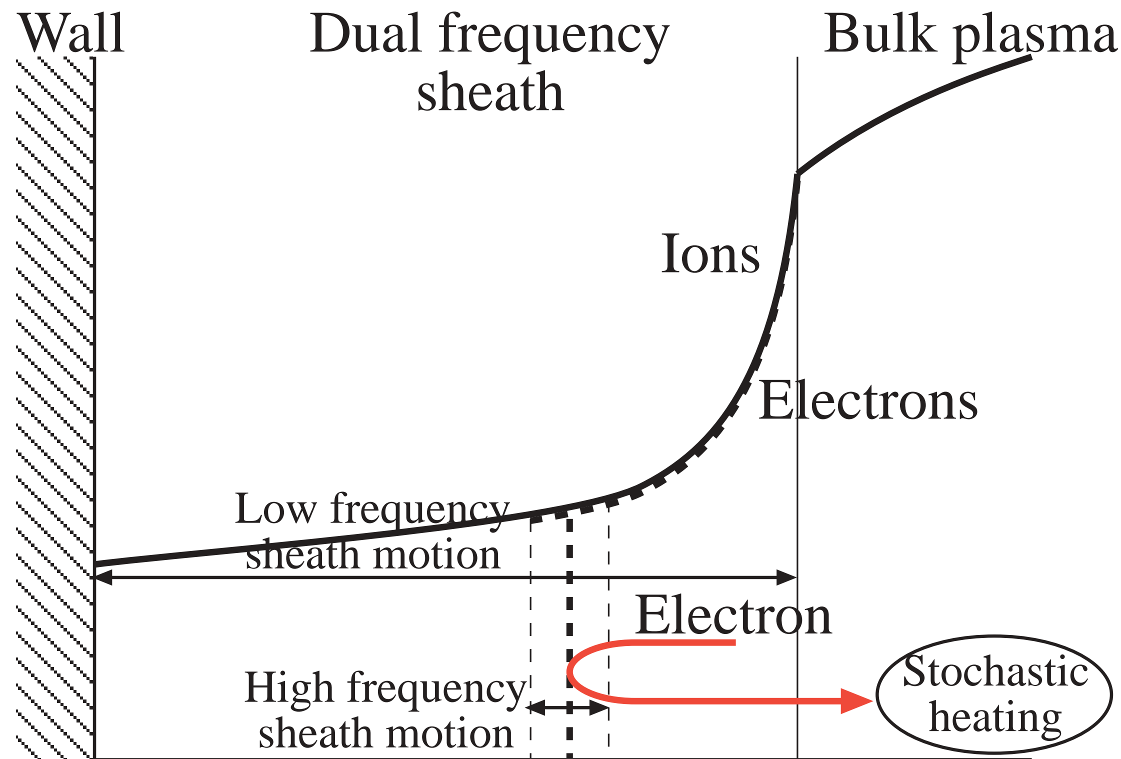
$$\boxed{\frac{\omega_h^2}{\omega_l^2} \gg \frac{V_l}{V_h} \gg 1}$$

H.C. Kim, J.K. Lee, and J.W. Shon, *Phys. Plasmas* **10**, 4545 (2003)
M.A. Lieberman, J. Kim, J.P. Booth, J.M. Rax and M.M. Turner, SEMICON Korea Etching Symposium, p. 23 (2003)
P.C. Boyle, A.R. Ellingboe, and M.M. Turner, *J. Phys. D: Appl. Phys.* **37**, 697 (2004)

ENERGY AND POWER DEPOSITION

1. DUAL FREQUENCY STOCHASTIC HEATING

- An important electron heating process below 100 mTorr



- How are electrons heated by the high frequency oscillations?

STOCHASTIC HEATING POWER

- Hard wall theory in dual frequency regime:

$$S_{\text{stoc}} = \underbrace{\frac{1}{2} m \bar{v}_e \frac{J_h^2}{e^2 n_s}}_{\text{High freq part}} \times \underbrace{\left(1 + \frac{\pi}{4} H_l\right) \left(\frac{H_l}{H_l + 2.2}\right)}_{\text{Low freq part } F(H_l)}$$

S_{stoc} = stochastic heating power per unit electrode area

m = electron mass

$\bar{v}_e = (8e\mathrm{T}_e/\pi m)^{1/2}$ = mean thermal electron speed

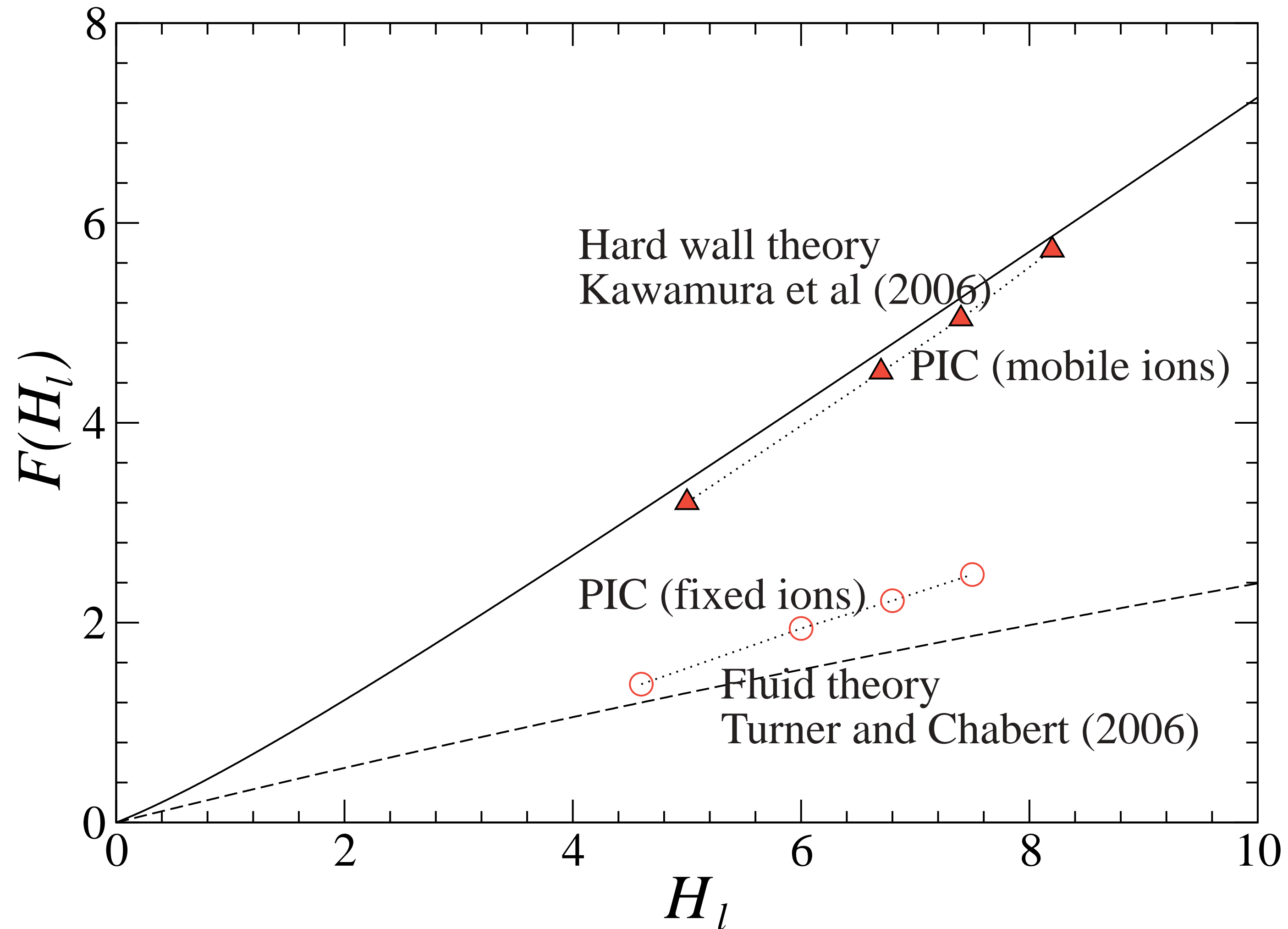
J_h = high frequency current density

n_s = plasma density at bulk plasma–sheath edge

$H_l = 0.55(V_l/\mathrm{T}_e)^{1/2}$ =low frequency enhancement factor

(E. Kawamura, M.A. Lieberman, and A.J. Lichtenberg, *Phys. Plasmas* **13,** 053506/1–14, 2006)

PARTICLE-IN-CELL SIMULATIONS



(M.M. Turner and P. Chabert, *Phys. Rev. Lett.* **96,** 205001/1–4, 2006)

2. COUPLING OF VOLTAGES

- The additive assumption for ion energy gives

$$\mathcal{E}_i \approx 0.41\,(V_l + V_h)$$

- Theoretical results give a cross term

$$\mathcal{E}_i \;\propto\; \left(V_l + V_h - \underbrace{\frac{2}{3}\frac{V_l V_h}{V_l + V_h}}_{\text{cross term}}\right)$$

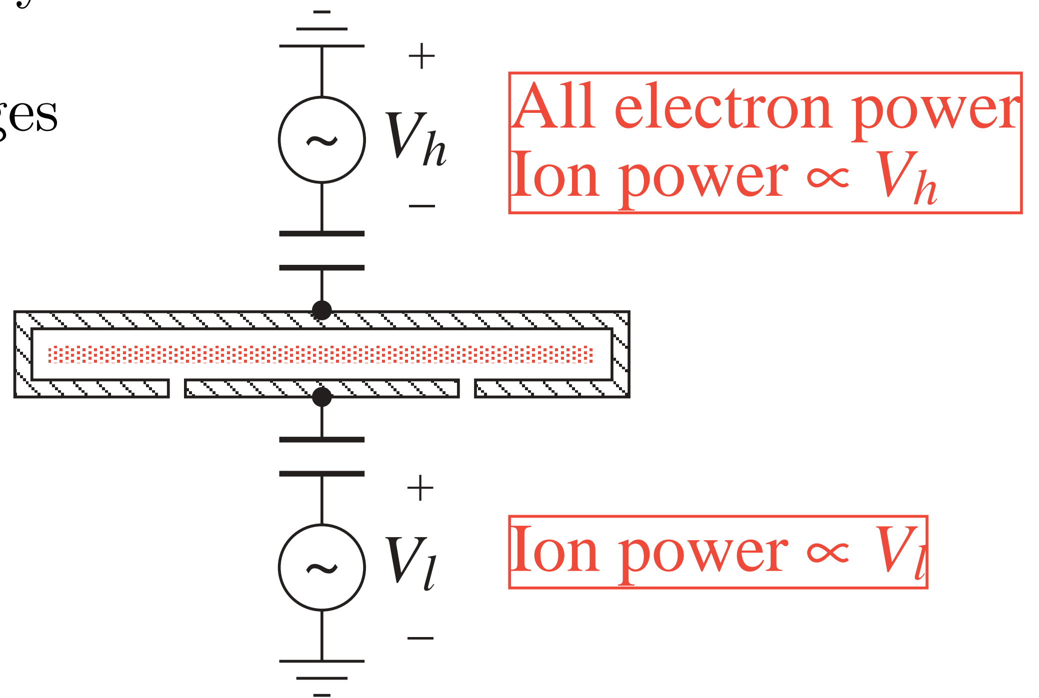
- A 17% worst-case effect when $V_l = V_h$

H.C. Kim, J.K. Lee, and J.W. Shon, *Phys. Plasmas* **10**, 4545 (2003)
P.C. Boyle, A.R. Ellingboe, and M.M. Turner, *J. Phys. D: Appl. Phys.* **37**, 697 (2004)

3. ION POWER SUPPLIED BY SOURCES

- High frequency source supplies electron power P_e
- Theory indicates that low and high frequency sources supply ion bombarding power P_i in proportion to their voltages

$$\frac{P_{il}}{P_{ih}} = \frac{V_l}{V_h}$$



STANDING WAVES AND SKIN EFFECTS

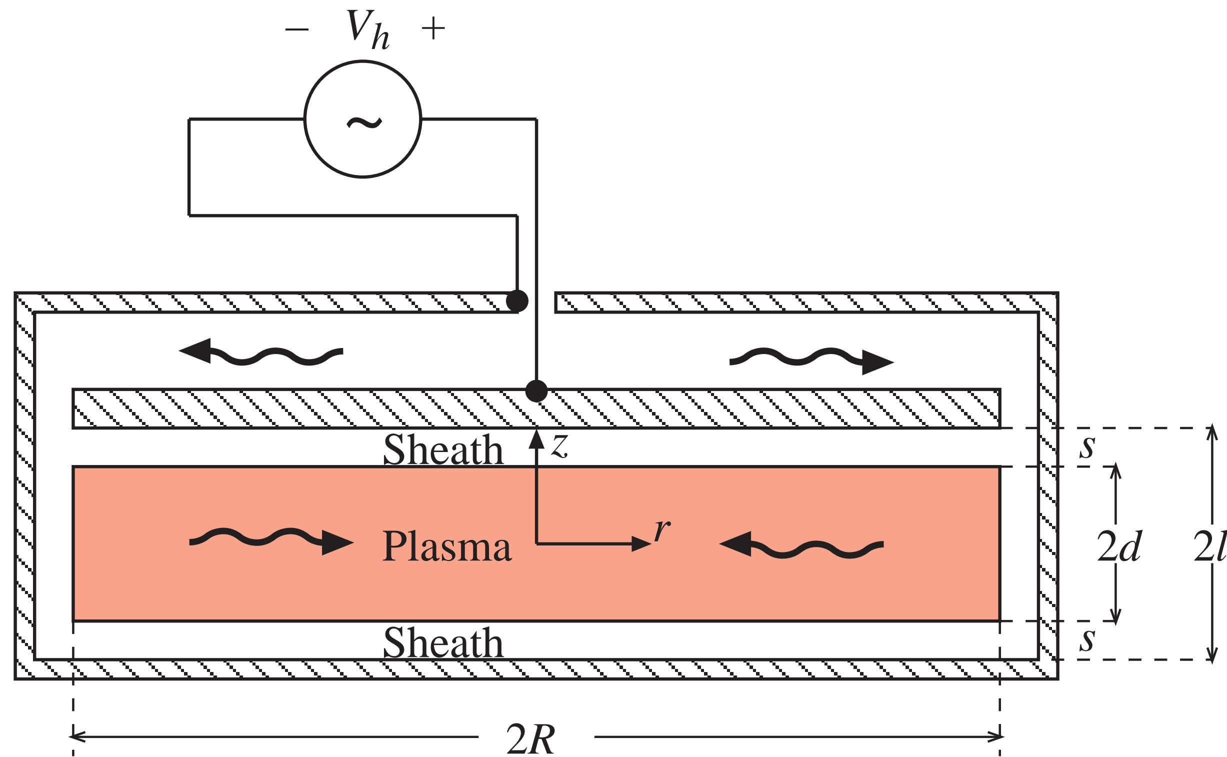
HIGH FREQUENCY ELECTROMAGNETIC EFFECTS

- High frequency and large area $\Rightarrow$ standing wave effects
- High frequency $\Rightarrow$ high density $\Rightarrow$ skin effects

M.A. Lieberman, J.P. Booth, P. Chabert, J.M. Rax, and M.M. Turner, *Plasma Sources Sci. Technol.* **11**, 283 (2002)

CYLINDRICAL CAPACITIVE DISCHARGE

Consider only the high frequency source

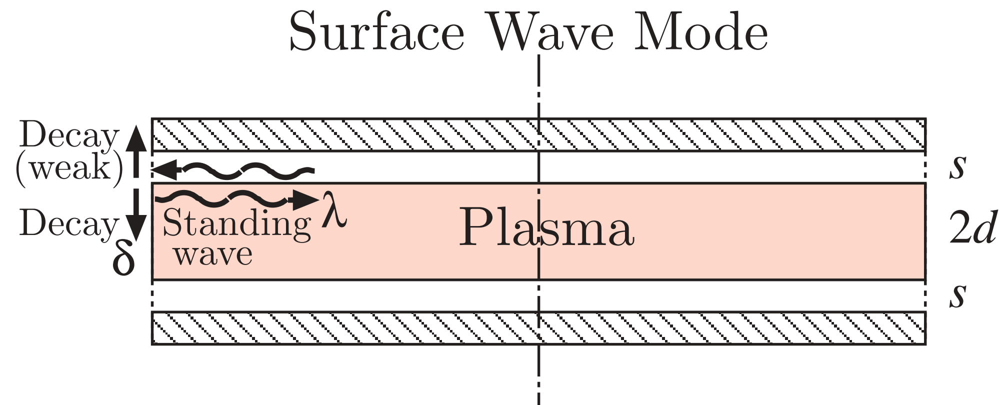


Fields cannot pass through metal plates

(1) V_s excites radially outward wave in top vacuum gap
(2) Outward wave excites radially inward wave in plasma

SURFACE WAVE MODE

- Power enters the plasma via a *surface wave mode:*



- Radial wavelength for surface wave (low density limit):

$$\lambda \approx \frac{\lambda_0}{\sqrt{1 + d/s}} \sim \frac{\lambda_0}{3}$$

with $\lambda_0 = c/f$ the free space wavelength

- Axial skin depth for surface wave:

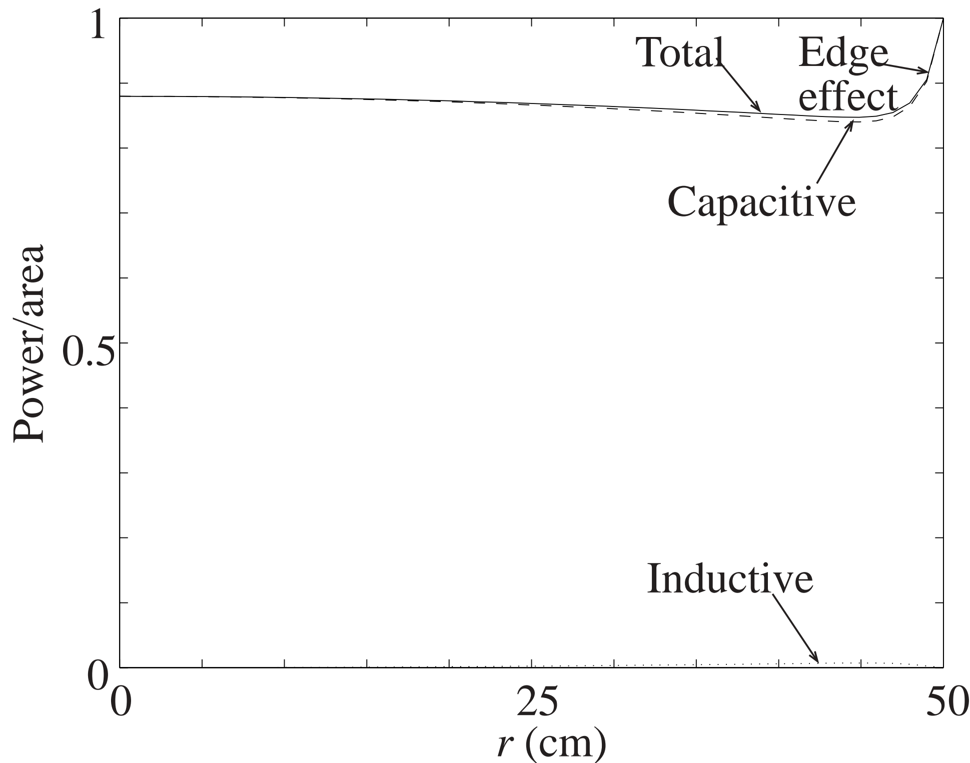
$$\delta \sim \frac{c}{\omega_p}$$

- There are also *evanescent modes* leading to edge effects near $r = R$

4. STANDING WAVE EFFECT

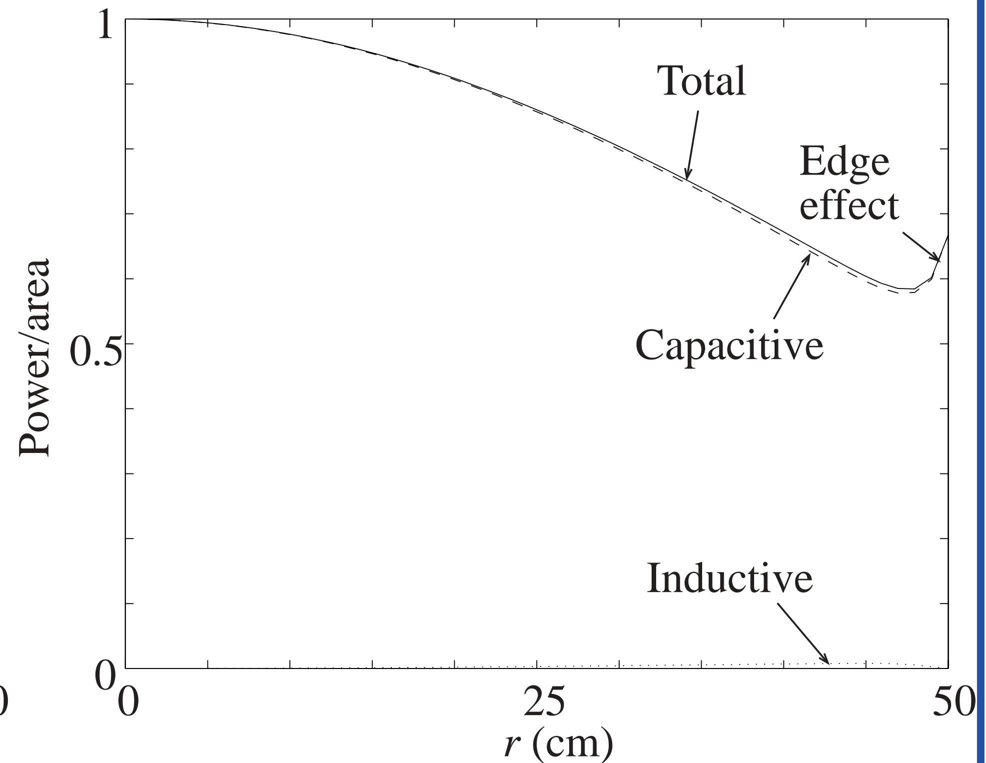
- $R = 50$ cm, $d = 2$ cm, $s = 0.4$ cm, $n_e = 10^9$ cm^{-3}, $\delta \approx 16$ cm
- $P_{\rm cap}$ (dash), $P_{\rm ind}$ (dot) and $P_{\rm tot}$ (solid) as a function of r

13.56 MHz ($\lambda \approx 9$–10 m)



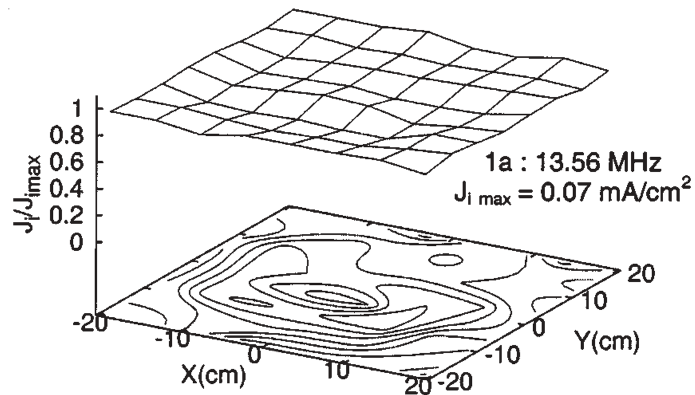
Small standing wave and skin effects

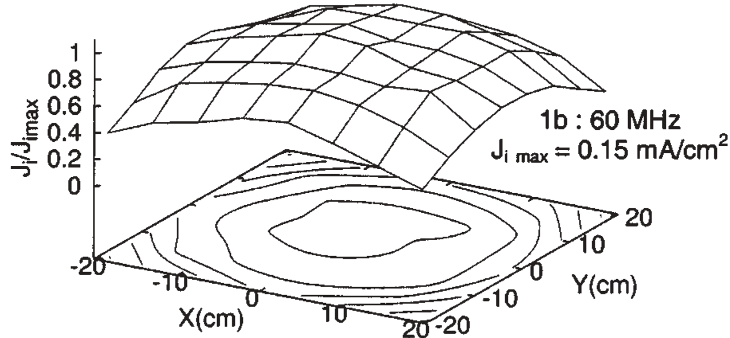
40.7 MHz ($\lambda \approx 3$ m)

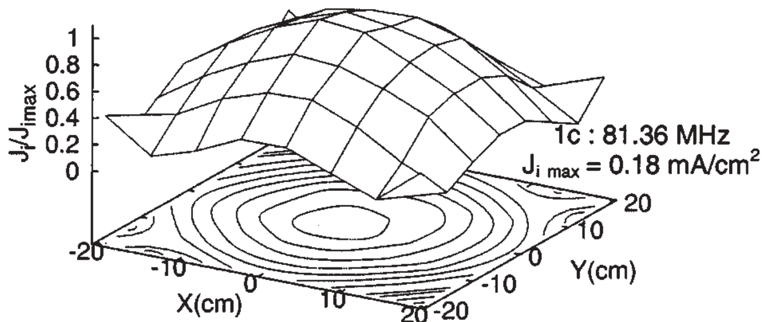


Large standing wave effect; center-high profile

EXPERIMENTAL RESULTS FOR STANDING WAVES







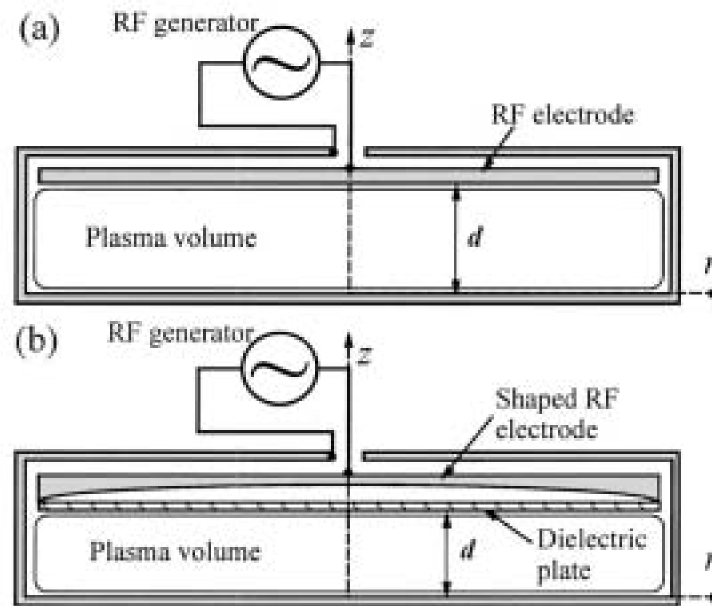
20×20 cm discharge
$p = 150$ mTorr
50 W rf power

The standing wave effect is seen at 60 MHz and is more pronounced at 81.36 MHz

(A. Perret, P. Chabert, J-P Booth, J. Jolly, J. Guillon and Ph. Auvray, *Appl. Phys. Lett.* **83**, 243, 2003)

SUPPRESSION OF STANDING WAVE EFFECTS

- Shaped electrode (and diel plate) eliminate standing wave effects



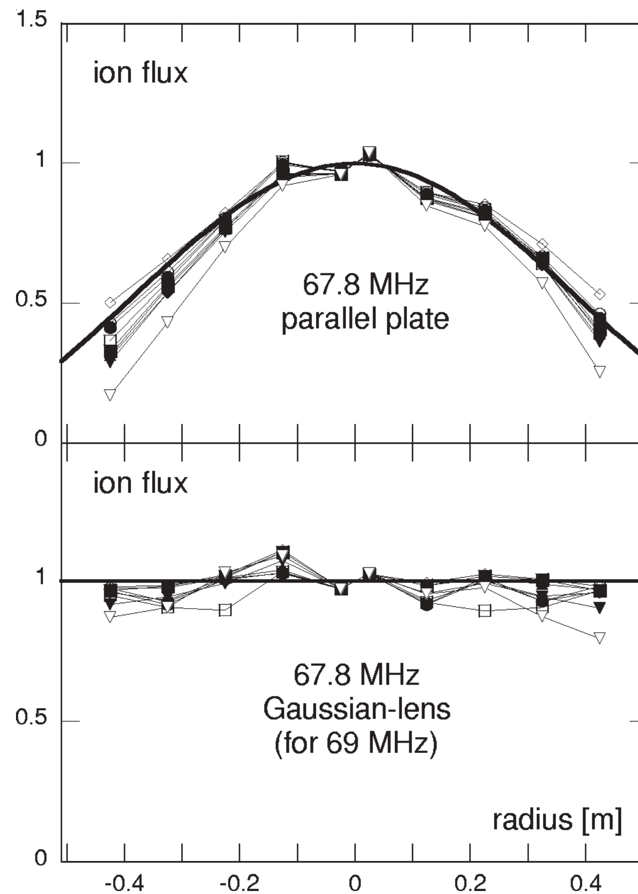
- Increased overall thickness in center compared to edge keeps voltage across discharge section constant
- The electrode shape is a Gaussian, independent of the plasma properties

L. Sansonnens and J. Schmitt, *Appl. Phys. Lett.* **82**, 182 (2003)

P. Chabert, J.L. Raimbault, J.M. Rax, and A. Perret, *Phys. Plasmas* **11**, 4081 (2004)

EXPERIMENTAL CONFIRMATION

- 5–250 mTorr argon, 50–300 W



H. Schmitt et al, *J. Appl. Phys.* **95**, 4559 (2004)

5. SKIN EFFECTS

- Skin effects $\Longrightarrow$ radial nonuniformities at high densities when

$$\boxed{\delta \lesssim 0.45\sqrt{d\,R}}$$

$\delta \propto \dfrac{1}{\sqrt{n}}$ = collisional or collisionless skin depth

d = bulk plasma half-thickness

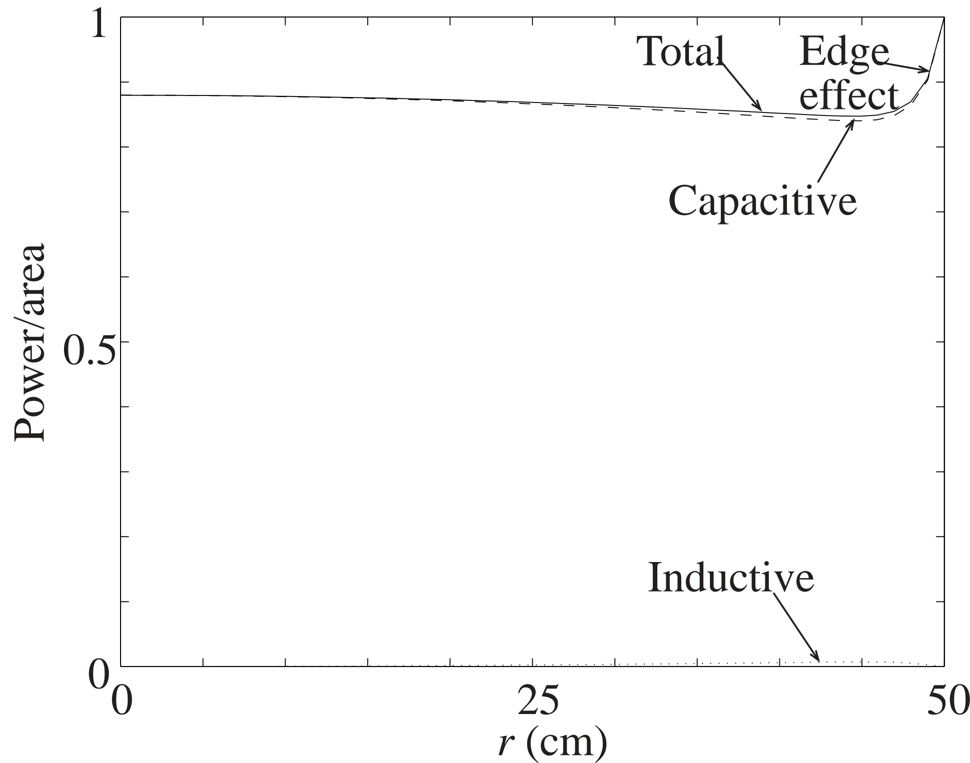
R = discharge radius

(P. Chabert, J.L. Raimbault, P. Levif, J.M. Rax, and M.A. Lieberman, *Plasma Sources: Sci. Technol.* **15,** S130–136, 2006)

SKIN EFFECTS

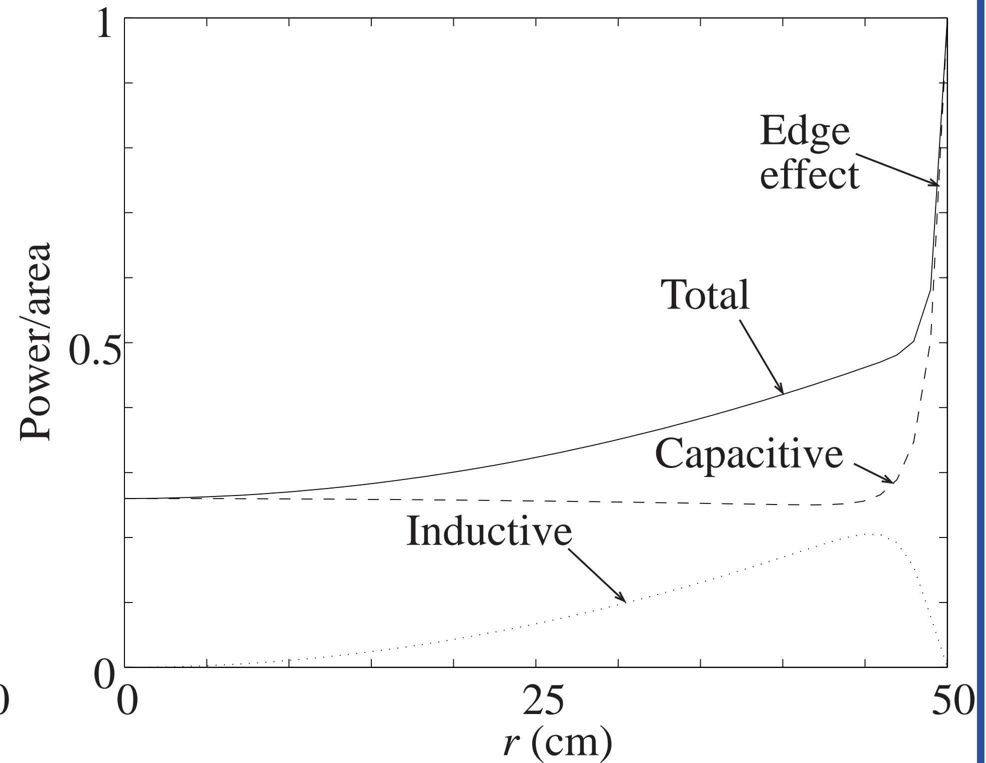
- $R = 50$ cm, $d = 2$ cm, $s = 0.4$ cm, $f = 13.56$ MHz, $\lambda \approx 9$ m
- P_{cap} (dash), P_{ind} (dot) and P_{tot} (solid) as a function of r

$\mathbf{n_e = 10^9\ cm^{-3}}$ ($\delta = 16.7$ cm)



Small standing wave and skin effects

$\mathbf{n_e = 10^{10}\ cm^{-3}}$ ($\delta = 5.3$ cm)



Large skin effects; center-low profile

THE NEXT 15 YEARS AND BEYOND

THE EXPERTS SPEAK†

- "There is not the slightest indication that [nuclear] energy will ever be obtained" — *Albert Einstein, 1932*
- "Anyone who expects a source of power from the transformation of these atoms is talking moonshine." — *Ernest Rutherford, 1933*
- "A few decades hence, [when controlled fusion is achieved], energy will be free — just like the unmetered air." — *John von Neumann, 1956*
- "Radio has no future." — *Lord Kelvin, 1897*
- "I think there is a world market for about five computers." — *Thomas J. Watson, 1943*
- Where a calculator like ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers in the future may have only 1,000 vacuum tubes and perhaps only weigh $1\frac{1}{2}$ tons." — *Popular Mechanics, March 1949*
- "640k ought to be enough for anybody." — *Bill Gates, 1981*

† C. Cerf and V. Navasky, Villard, New York, 1998

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS (ITRS 2005)

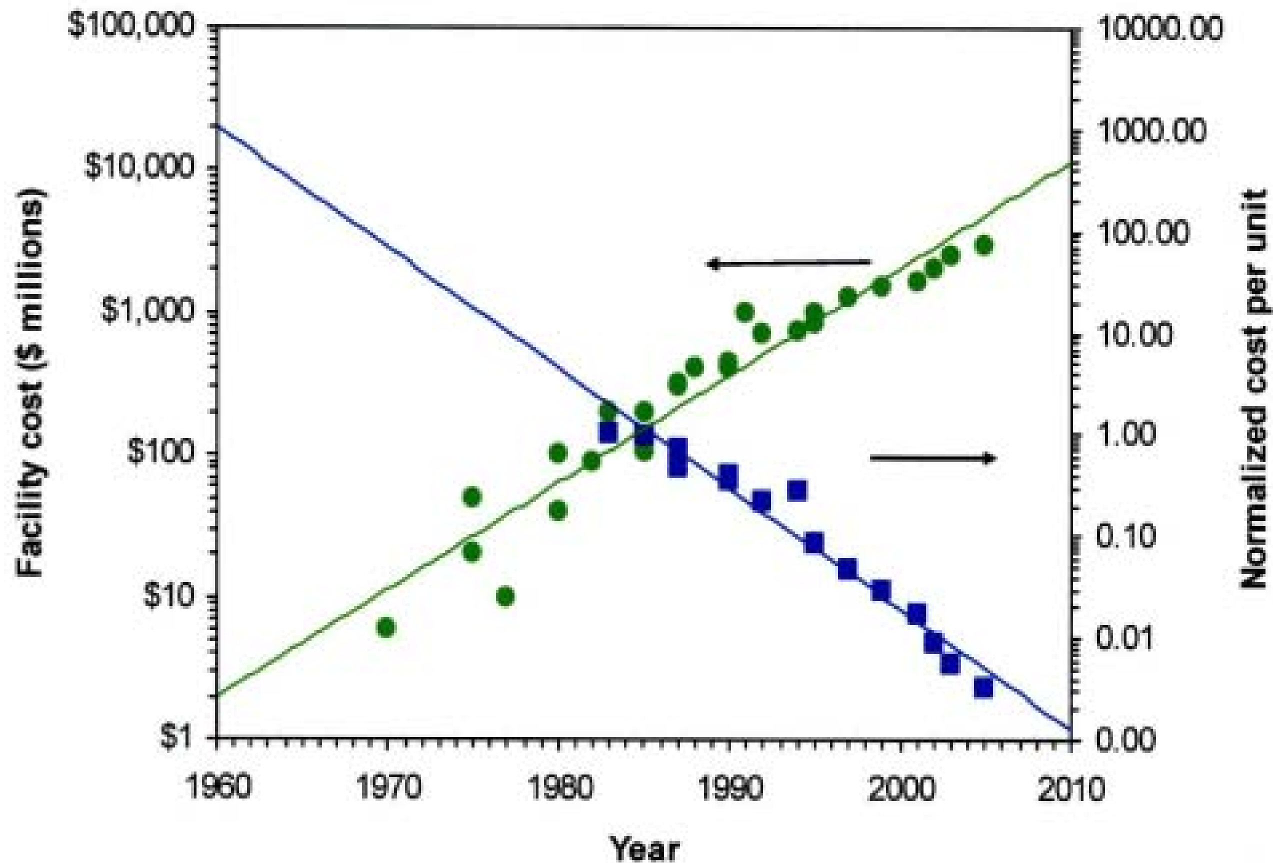
Year	2006	2009	2011	2013	2015	2017	2020
Half-pitch (nm)	70	50	40	32	25	20	14
Gate length (nm)	28	20	16	13	10	8	6

- Below limits imposed by thermodynamics and quantum mechanics
- Major issues are transistor physics, materials limitations, and power dissipation
  - Doping profiles, silicon-on-insulator, FinFET's, tri-gate structures
  - High-κ gate dielectrics, metal gates, strained Si, Si-Ge, low-κ interconnect dielectrics
  - Power limitation of around 200 W/cm^2
- Formidable manufacturing issues remain; eg, lithography, metrology

> "You can scale CMOS down another 10–15 years; nothing touches the economics of it." — Intel CEO Craig Barrett

COST OF FABS

- Cost of fabs is growing exponentially ($3–4 billion/fab in 2006)



- But cost per unit output is falling exponentially!

Fabs are becoming more economical

BEYOND 2020

- Moore's law (miniaturization) ends, but products improve for many years
- MOS-FET's continue for fast switches

  Vertical CMOS transistors $\rightarrow$ silicon/carbon nanowires/nanotubes?
- Copper/low-κ dielectric layers continue for interconnects

  Copper $\rightarrow$ carbon nanotubes? Optical interconnects?
- CMOS memory migrates to compatible magnetic memory

  "Spintronics:" electron charge $\rightarrow$ electron spin

  Flash (slow) and DRAM (volatile) $\rightarrow$ MRAM (fast, non-volatile)?

  $\Rightarrow$ 1st product in 2006: Freescale MRAM (4 Mb, 35 ns)

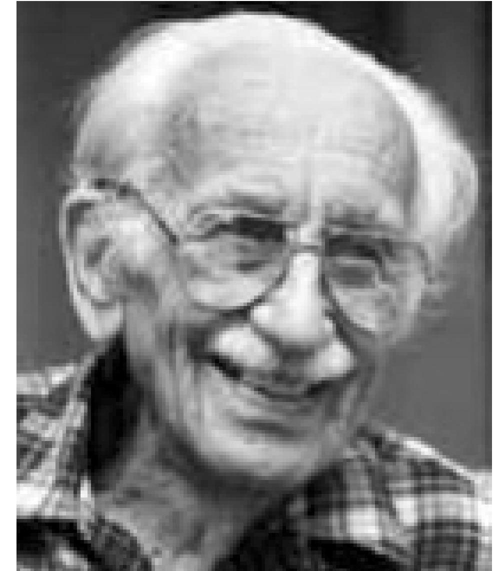
PIE IN THE SKY†

- "3D chips" (heat removal limit of 200 W/cm^2)
- "Single-molecule transistors" (not much smaller than CMOS transistors)
- "Single-electron transistors" (need very low temperatures)
- "Cross-bar computing" (replace reliable CMOS switches with defect-prone nanowire switches)
- "Self-assembled, DNA-based computers" (we each own one already)
- "Quantum computing using qubits" (exponentially faster computation for niche applications)

† From a Joe Hill union song, *The Preacher and the Slave*, 1911

CONCLUSIONS

- CMOS scales to 24-atom gate lengths in 2020
- CMOS product improvements continue far beyond 2020
- Plasma reactor research and development will intensify to meet these needs
- Displacing CMOS beyond 2020 is unlikely; instead, other technologies will be integrated into the CMOS platform



W.P. Allis (1901–1999)
Co-founder of the GEC

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