The DASH Prototype: Implementation and Performance
Authors: D. Lenoski et. al.

Mel Tsai, CS 258
3/20/02

DASH Processing Node
- Four processors per node
- Snoopy caches, MESI protocol (cache-cache xfers)
- Grouped for locality and to aggregate Directory logic
- Release consistency (full & write fences), non-binding prefetch
- Retry masking within node: split-transaction

DASH Memory Hierarchy
- Processor Level
- Local Cluster Level
- Directory Home Level
- Remote Cluster Level

DASH Processing Node
- MIPS R3000
- L1/L2 Caches

DASH Memory Hierarchy
- Processor Level
- Local Cluster Level
- Directory Home Level
- Remote Cluster Level

The DASH Prototype
- Sixteen 33 MHz MIPS R3000’s, up to 64 possible due to memory addressability
- L1: 64 Kbyte I & D per processor
- L2: 256 Kbyte write-back
- "DC" and "RC" boards comprise directory logic for each node
- Request-reply mesh network, wormhole routed
Directory-based Coherence

- Distributed directories, P2P invalidation with ACKs
- Directory pointers are 16-bit vectors implemented using DRAM
- One bit indicates cached/uncached for each node
- Additional state bit indicates shared/dirty
- Remote Access Cache (RAC) buffers and coordinates external requests

Directory Logic

Performance Monitoring

- Significant resources dedicated to performance monitoring
- Implements both event counters and bus tracing
- Configured through a Xilinx FPGA

Low-level DASH Performance
Speedups (sort-of)