Recall: Data Hazard Solution: Forwarding

- “Forward” result from one stage to another

Recall: Resolve RAW by “forwarding” (or bypassing)

- Detect nearest valid write op operand register and forward into op latches, bypassing remainder of the pipe
- Increase muxes to add paths from pipeline registers
- Data Forwarding = Data Bypassing

FYI: MIPS R3000 clocking discipline

- 2-phase non-overlapping clocks
- Pipeline stage is two (level sensitive) latches

Edge-triggered
MIPS R3000 Instruction Pipeline

<table>
<thead>
<tr>
<th>Inst Fetch</th>
<th>Decode</th>
<th>Reg. Read</th>
<th>ALU / E.A</th>
<th>Memory</th>
<th>Write Reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLB</td>
<td>I-Cache</td>
<td>RF</td>
<td>Operation</td>
<td>E.A</td>
<td>TLB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>D-Cache</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Resource Usage

TLB | TLB | I-cache | RF | ALU | ALU | D-Cache | WB

Write in phase 1, read in phase 2 => eliminates bypass from WB

Thus, only 2 levels of forwarding

Time (clock cycles)

IF  ID/RF  EX  MEM  WB

with MIPS R3000 pipeline, no need to forward from WB stage

Recall: Examples of stalls/bubbles

- Exceptions: Flush everything above
  - Prevent instructions following exception from committing state
  - Freeze fetch until exception resolved

- Stalls: Introduce brief stalls into pipeline
  - Decode stage recognizes that current instruction cannot proceed
  - Freeze fetch stage
  - Introduce “bubble” into EX stage (instead of forwarding stalled inst)
  - Can stall until condition is resolved
  - Examples:
    - mfhi, mflo: need to wait for multiply/divide unit to finish
    - “Break” instruction for Lab5: stall until release line received
    - Load delay slot handled this way as well

Recall: Freeze above & Bubble Below

Flush accomplished by setting “invalid” bit in pipeline
Recall: Achieving Precise Exceptions

- Use pipeline to sort this out!
  - Pass exception status along with instruction.
  - Keep track of PCs for every instruction in pipeline.
  - Don’t act on exception until it reach WB stage

- Handle interrupts through “faulting noop” in IF stage
- When instruction reaches end of MEM stage:
  - Save PC ⇒ EPC, Interrupt vector addr ⇒ PC
  - Turn all instructions in earlier stages into noops!

Recall: What about memory operations?

- If instructions are initiated in order and operations always occur in the same stage, there can be no hazards between memory operations!

- What about data dependence on loads?
  R1 ← R4 + R5
  R2 ← Mem[R2 + I]
  R3 ← R2 + R1
  ⇒ “Delayed Loads”

- Can recognize this in decode stage and introduce bubble while stalling fetch stage (hint for lab 4!)

- Tricky situation:
  R1 ← Mem[R2 + I]
  Mem[R3+34] ← R1
  Handle with bypass in memory stage!

MIPS R3000 Multicycle Operations

- Use control word of local stage to step through multicycle operation

- Stall all stages above multicycle operation in the pipeline

- Drain (bubble) stages below it

- Alternatively, launch multiply/divide to autonomous unit, only stall pipe if attempt to get result before ready

- This means stall mflo/mfhi in decode stage if multiply/divide still executing
- Extra credit in Lab 5 does this

Case Study: MIPS R4000 (200 MHz)

- 8 Stage Pipeline:
  - IF–first half of fetching of instruction; PC selection happens here as well as initiation of instruction cache access.
  - IS–second half of access to instruction cache.
  - RF–instruction decode and register fetch, hazard checking and also instruction cache hit detection.
  - EX–execution, which includes effective address calculation, ALU operation, and branch target computation and condition evaluation.
  - DF–data fetch, first half of access to data cache.
  - DS–second half of access to data cache.
  - TC–tag check, determine whether the data cache access hit.
  - WB–write back for loads and register-register operations.

- 8 Stages:
  What is impact on Load delay? Branch delay? Why?
Case Study: MIPS R4000

TWO Cycle Load Latency

IF IS RF EX DF DS TC WB
IF IS RF EX DF DS TC
IF IS RF EX DF DS TC
IF IS RF EX DF
IF IS RF
IF IS

THREE Cycle Branch Latency

IF IS RF EX DF DS TC WB
IF IS RF EX DF DS TC
IF IS RF EX DF DS TC
IF IS RF EX DF
IF IS RF
IF IS

MIPS R4000 Floating Point

° FP Adder, FP Multiplier, FP Divider
° Last step of FP Multiplier/Divider uses FP Adder HW
° 8 kinds of stages in FP units:

<table>
<thead>
<tr>
<th>Stage</th>
<th>Functional unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>FP adder</td>
<td>Mantissa ADD stage</td>
</tr>
<tr>
<td>D</td>
<td>FP divider</td>
<td>Divide pipeline stage</td>
</tr>
<tr>
<td>E</td>
<td>FP multiplier</td>
<td>Exception test stage</td>
</tr>
<tr>
<td>M</td>
<td>FP multiplier</td>
<td>First stage of multiplier</td>
</tr>
<tr>
<td>N</td>
<td>FP multiplier</td>
<td>Second stage of multiplier</td>
</tr>
<tr>
<td>R</td>
<td>FP adder</td>
<td>Rounding stage</td>
</tr>
<tr>
<td>S</td>
<td>FP adder</td>
<td>Operand shift stage</td>
</tr>
<tr>
<td>U</td>
<td>Unpack FP numbers</td>
<td></td>
</tr>
</tbody>
</table>

MIPS FP Pipe Stages

| FP Instr   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | ...
<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Add, Subtract</td>
<td>U</td>
<td>S+A</td>
<td>A+R</td>
<td>R+S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multiply</td>
<td>U</td>
<td>E+M</td>
<td>M</td>
<td>M</td>
<td>M</td>
<td>N</td>
<td>N+A</td>
<td>R</td>
<td></td>
</tr>
<tr>
<td>Divide</td>
<td>U</td>
<td>A</td>
<td>R</td>
<td>D^2</td>
<td>...</td>
<td>D+A</td>
<td>D+R,R</td>
<td>D+A</td>
<td>D+R,A</td>
</tr>
<tr>
<td>Square root</td>
<td>U</td>
<td>E</td>
<td>(A+R)</td>
<td>108</td>
<td>...</td>
<td>A</td>
<td>R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negate</td>
<td>U</td>
<td>S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Absolute value</td>
<td>U</td>
<td>S</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FP compare</td>
<td>U</td>
<td>A</td>
<td>R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Stages:</td>
<td>M</td>
<td>First stage of multiplier</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>N</td>
<td>Second stage of multiplier</td>
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<tr>
<td></td>
<td>R</td>
<td>Rounding stage</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>S</td>
<td>Operand shift stage</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Recall: Compute CPI?

° Start with Base CPI
° Add stalls

\[
CPI = CPI_{base} + CPI_{stall}
\]

\[
CPI_{stall} = STALL_{type-1} \times freq_{type-1} + STALL_{type-2} \times freq_{type-2}
\]

° Suppose:
  • CPI_{base} = 1
  • Freq\text{branch}=20\%, freq\text{load}=30\%
  • Suppose branches always cause 1 cycle stall
  • Loads cause a 100 cycle stall 1% of time
° Then: \( CPI = 1 + (1\times0.20) + (100 \times 0.30\times0.01) = 1.5 \)
° Multicycle? Could treat as:

\[
CPI_{stall} = (CYCLES-CPI_{base}) \times freq_{inst}
\]
**R4000 Performance**

- Not ideal CPI of 1:
  - FP structural stalls: Not enough FP hardware (parallelism)
  - FP result stalls: RAW data hazard (latency)
  - Branch stalls: 2 cycles + unfilled slots
  - Load stalls: 1 or 2 clock cycles

**Administrivia**

- Midterm almost graded
  - This test was too long! (Sorry)
  - More on Wednesday
- Should start working on Lab 4!
  - Remember: a Working processor is necessary for full credit...
  - Due Tonight: Problem 0 (Lab evaluation of Lab 4)
  - Due Tomorrow night: Division of labor for Lab 5
- Get started early!!!
- Wednesday night: Your design document due
  - Discuss them in section on Thursday
  - Final due Thursday at Midnight
- More info on advanced topics:
  - Computer Architecture: A Quantitative Approach by John Hennessy and David Patterson
  - Should be on reserve at Engineering library

**Administrivia: Pentium-4 Architecture!**

- Microprocessor Report: August 2000
  - 20 Pipeline Stages!
  - Drive ⇒ Wire Delay!
  - Trace-Cache: caching paths through the code for quick decoding.
  - Renaming: similar to Tomasulo architecture
  - Branch and DATA prediction!

**Can we somehow make CPI closer to 1?**

- Let’s assume full pipelining:
  - If we have a 4-cycle instruction, then we need 3 instructions between a producing instruction and its use:

```
multf $F0,$F2,$F4
delay-1
delay-2
delay-3
addf $F6,$F10,$F0
```

- Earliest forwarding for 4-cycle instructions
- Earliest forwarding for 1-cycle instructions
FP Loop: Where are the Hazards?

Loop:

1. LD F0,0(R1); F0=vector element
2. ADDD F4,F0,F2; add scalar from F2
3. SD 0(R1),F4; store result
4. SUBI R1,R1,8; decrement pointer 8B (DW)
5. BNEZ R1,Loop; branch R1!=zero
6. NOP; delayed branch slot

Where are the stalls?

- Instruction
  - FP ALU op
  - Load double
  - Integer op
- Instruction Latency in producing result using result clock cycles
  - FP ALU op
  - Load double
  - Integer op
  - 0

FP Loop Showing Stalls

1. Loop: LD F0,0(R1); F0=vector element
2. stall
3. ADDD F4,F0,F2; add scalar from F2
4. stall
5. stall
6. SD 0(R1),F4; store result
7. SUBI R1,R1,8; decrement pointer 8B (DW)
8. BNEZ R1,Loop; branch R1!=zero
9. stall; delayed branch slot

Where are the stalls?

- Instruction
  - FP ALU op
  - Load double
  - Integer op
- Instruction Latency in producing result using result clock cycles
  - FP ALU op
  - Load double
  - Integer op
  - 0

9 clocks: Rewrite code to minimize stalls?

- Swap BNEZ and SD by changing address of SD
  - Instruction
    - FP ALU op
    - Load double
  - Instruction Latency in producing result using result clock cycles
    - FP ALU op
    - Load double
  - 0

Revised FP Loop Minimizing Stalls

1. Loop: LD F0,0(R1)
2. stall
3. ADDD F4,F0,F2
4. SUBI R1,R1,8
5. BNEZ R1,Loop; delayed branch
6. SD 8(R1),F4; altered when move past SUBI

Unroll Loop Four Times (straightforward way)

1. Loop: LD F0,0(R1)
2. ADDD F4,F0,F2
3. SD 0(R1),F4; drop SUBI & BNEZ
4. LD F6,-8(R1)
5. ADDD F8,F6,F2
6. SD -8(R1),F8; drop SUBI & BNEZ
7. LD F10,-16(R1)
8. ADDD F12,F10,F2
9. SD -16(R1),F12; drop SUBI & BNEZ
10. LD F14,-24(R1)
11. ADDD F16,F14,F2
12. SD -24(R1),F16
13. SUBI R1,R1,#32; alter to 4*8
14. BNEZ R1,LOOP
15. NOP

Rewrite loop to minimize stalls?

1 cycle stall
2 cycles stall

6 clocks: Unroll loop 4 times code to make faster?

15 + 4 x (1+2) = 27 clock cycles, or 6.8 per iteration
Assumes R1 is multiple of 4
CPI = 27/15 = 1.8
What assumptions made when moved code?

- OK to move store past SUBI even though changes register
- OK to move loads before stores: get right data?
- When is it safe for compiler to do such changes?

1 Loop:

1. LD    F0,0 (R1)
2. LD    F6,-8 (R1)
3. LD    F10,-16 (R1)
4. LD    F14,-24 (R1)
5. ADDD F4,F0,F2
6. ADDD F8,F6,F2
7. ADDD F12,F10,F2
8. ADDD F16,F14,F2
9. SD    0 (R1), F4
10. SD   -8 (R1), F8
11. SD  -16 (R1), F12
12. SUBI R1,R1,#32
13. BNEZ R1, LOOP
14. SD    8 (R1), F16 ; 8-32 = -24

14 clock cycles, or 3.5 per iteration
CPI = 14/14 = 1

When safe to move instructions?

Two main variations: Superscalar and VLIW

- Superscalar: varying no. instructions/cycle (1 to 6)
  - Parallelism and dependencies determined/resolved by HW
  - IBM PowerPC 604, Sun UltraSparc, DEC Alpha 21164, HP 7100
- Very Long Instruction Words (VLIW): fixed number of instructions (16) parallelism determined by compiler
  - Pipeline is exposed; compiler must schedule delays to get right result
- Explicit Parallel Instruction Computer (EPIC)/ Intel
  - 128 bit packets containing 3 instructions (can execute sequentially)
  - Can link 128 bit packets together to allow more parallelism
  - Compiler determines parallelism, HW checks dependencies and forwards/stalls

Unrolled Loop That Minimizes Stalls

Getting CPI < 1: Issuing Multiple Instructions/Cycle

- Superscalar DLX: 2 instructions, 1 FP & 1 anything else
  - Fetch 64-bits/clock cycle; Int on left, FP on right
  - Can only issue 2nd instruction if 1st instruction issues
  - More ports for FP registers to do FP load & FP op in a pair

<table>
<thead>
<tr>
<th>Type</th>
<th>PipeStages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int. instruction</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>FP instruction</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>Int. instruction</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>FP instruction</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>FP instruction</td>
<td>IF ID EX MEM WB</td>
</tr>
</tbody>
</table>

- 1 cycle load delay expands to 3 instructions in SS
  - instruction in right half can’t use it, nor instructions in next slot

Unrolled 5 times to avoid delays (+1 due to SS)

- 12 clocks, or 2.4 clocks per iteration

Getting CPI < 1: Issuing Multiple Instructions/Cycle

- Two main variations: Superscalar and VLIW

- Superscalar: varying no. instructions/cycle (1 to 6)
  - Parallelism and dependencies determined/resolved by HW
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  - Pipeline is exposed; compiler must schedule delays to get right result

- Explicit Parallel Instruction Computer (EPIC)/ Intel
  - 128 bit packets containing 3 instructions (can execute sequentially)
  - Can link 128 bit packets together to allow more parallelism
  - Compiler determines parallelism, HW checks dependencies and forwards/stalls
Limits of Superscalar

- While Integer/FP split is simple for the HW, get CPI of 0.5 only for programs with:
  - Exactly 50% FP operations
  - No hazards

- If more instructions issue at same time, greater difficulty of decode and issue
  - Even 2-scalar => examine 2 opcodes, 6 register specifiers, & decide if 1 or 2 instructions can issue

- VLIW: tradeoff instruction space for simple decoding
  - The long instruction word has room for many operations
  - By definition, all the operations the compiler puts in the long instruction word can execute in parallel
  - E.g., 2 integer operations, 2 FP ops, 2 Memory refs, 1 branch
  - 16 to 24 bits per field => 7*16 or 112 bits to 7*24 or 168 bits wide
  - Need compiling technique that schedules across several branches

Loop Unrolling in VLIW

<table>
<thead>
<tr>
<th>Memory reference 1</th>
<th>Memory reference 2</th>
<th>FP operation 1</th>
<th>FP op. 2</th>
<th>Int. op/ branch</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F0,0(R1)</td>
<td>LD F6,-8(R1)</td>
<td>ADDD F4, F0, F2</td>
<td>ADDD F8,F6,F2</td>
<td>ADDD F16,F14,F2</td>
<td>1</td>
</tr>
<tr>
<td>LD F18,-32(R1)</td>
<td>LD F22,-40(R1)</td>
<td>ADDD F10,F2 ADDD F16,F22,F2</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LD F26,-48(R1)</td>
<td>ADDD F18,F14,F2</td>
<td>ADDD F20, F18, F2 ADDD F24,F22,F2</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD 0(R1),F4</td>
<td>SD -8(R1),F8</td>
<td>ADDD F28, F26, F2</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD -16(R1),F16</td>
<td>SD -24(R1),F16</td>
<td>ADDD F28, F26, F2</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD -32(R1),F20</td>
<td>SD -40(R1),F24</td>
<td>SUBI R1,R1,#48</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD -0(R1),F28</td>
<td>BNEZ R1,LOOP</td>
<td>BNEZ R1,LOOP</td>
<td>7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unrolled 7 times to avoid delays
7 results in 9 clocks, or 1.3 clocks per iteration

Need more registers in VLIW(EPIC => 128int + 128FP)

Software Pipelining

- Observation: if iterations from loops are independent, then can get more ILP by taking instructions from different iterations

- Software pipelining: reorganizes loops so that each iteration is made from instructions chosen from different iterations of the original loop (- Tomasulo in SW)

- Symbolic Loop Unrolling
  - Maximize result-use distance
  - Less code space than unrolling
  - Fill & drain pipe only once per loop vs. once per each unrolled iteration in loop unrolling

Software Pipelining Example

Before: Unrolled 3 times

1. LD F0,0(R1)
2. ADDD F4,F0,F2
3. SD 0(R1),F4
4. LD F6,-8(R1)
5. ADDD F8,F6,F2
6. SD -8(R1),F8
7. LD F10,-16(R1)
8. ADDD F12,F10,F2
9. SD -16(R1),F12
10. SUBI R1,R1,#24
11. BNEZ R1,LOOP

After: Software Pipelined

1. SD 0(R1),F4 ; Stores M[i]
2. ADDD F4,F0,F2 ; Adds to M[i-1]
3. LD F0,-16(R1); Loads M[i-2]
4. SUBI R1,R1,#8
5. BNEZ R1,LOOP

Symbolic Loop Unrolling

- Maximize result-use distance
- Less code space than unrolling
- Fill & drain pipe only once per loop vs. once per each unrolled iteration in loop unrolling
Software Pipelining with Loop Unrolling in VLIW

<table>
<thead>
<tr>
<th>Memory reference 1</th>
<th>Memory reference 2</th>
<th>FP operation 1</th>
<th>FP operation 2</th>
<th>Int. op/ branch</th>
<th>Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F0,-48(R1)</td>
<td>ST 0(R1),F4</td>
<td>ADDD F4,F0,F2</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>LD F6,-56(R1)</td>
<td>ST -8(R1),F8</td>
<td>ADDD F8,F6,F2</td>
<td>SUBI R1,R1,#24</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>LD F10,-40(R1)</td>
<td>ST 8(R1),F12</td>
<td>ADDD F12,F10,F2</td>
<td></td>
<td>BNEZ R1,LOOP</td>
<td>3</td>
</tr>
</tbody>
</table>

° Software pipelined across 9 iterations of original loop
  • In each iteration of above loop, we:
    - Store to m,m-8,m-16 (iterations I-3,I-2,I-1)
    - Compute for m-24,m-32,m-40 (iterations I+1,I+2)
    - Load from m-48,m-56,m-64 (iterations I+3,I+4,I+5)

° 9 results in 9 cycles, or 1 clock per iteration
° Average: 3.3 ops per clock, 66% efficiency
Note: Need less registers for software pipelining
  (only using 7 registers here, was using 15)

Can we use HW to get CPI closer to 1?
° Why in HW at run time?
  • Works when can’t know real dependence at compile time
  • Compiler simpler
  • Code for one machine runs well on another

° Key idea: Allow instructions behind stall to proceed:
  DIVD F0,F2,F4
  ADDD F10,F0,F8
  SUBD F12,F8,F14

° Out-of-order execution => out-of-order completion.
° Disadvantages?
  • Complexity
  • Precise interrupts harder! (Talk about this next time)

Problems?
° How do we prevent WAR and WAW hazards?
° How do we deal with variable latency?
  • Forwarding for RAW hazards harder.

Clock Cycle Number

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Clock Cycle Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD F6,34(R2)</td>
<td>1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17</td>
</tr>
<tr>
<td>LD F2,45(R3)</td>
<td></td>
</tr>
<tr>
<td>MULD F0,F2,F4</td>
<td>IF ID EX MEM WB</td>
</tr>
<tr>
<td>SUBD F8,F6,F2</td>
<td>IF ID stall M1 M2 M3 M4 M5 M6 M7 M8 M9 M10 MEM WB</td>
</tr>
<tr>
<td>DIVD F10,F0,F6</td>
<td>IF ID stall stall stall stall stall stall stall D1 D2</td>
</tr>
<tr>
<td>ADDD F6,F8,F2</td>
<td>IF ID AL A2 MEM WB</td>
</tr>
</tbody>
</table>

RAW

WAR

The Big Picture: Where are We Now?
° The Five Classic Components of a Computer

° Today’s Topics:
  • Recap last lecture
  • Hardware loop unrolling with Tomasulo algorithm
  • Administrivia
  • Speculation, branch prediction
  • Reorder buffers
Scoreboard: a bookkeeping technique

- Out-of-order execution divides ID stage:
  1. Issue—decode instructions, check for structural hazards
  2. Read operands—wait until no data hazards, then read operands

- Scoreboards date to CDC6600 in 1963

- Instructions execute whenever not dependent on previous instructions and no hazards.

- CDC 6600: In order issue, out-of-order execution, out-of-order commit (or completion)
  - No forwarding!
  - Imprecise interrupt/exception model for now

Scoreboard Architecture (CDC 6600)

Scoreboard Implications

- Out-of-order completion => WAR, WAW hazards?

- Solutions for WAR:
  - Stall writeback until registers have been read
  - Read registers only during Read Operands stage

- Solution for WAW:
  - Detect hazard and stall issue of new instruction until other instruction completes

- No register renaming!

- Need to have multiple instructions in execution phase => multiple execution units or pipelined execution units

- Scoreboard keeps track of dependencies between instructions that have already issued.

- Scoreboard replaces ID, EX, WB with 4 stages

Four Stages of Scoreboard Control

- Issue—decode instructions & check for structural hazards (ID1)
  - Instructions issued in program order (for hazard checking)
  - Don’t issue if structural hazard
  - Don’t issue if instruction is output dependent on any previously issued but uncompleted instruction (no WAW hazards)

- Read operands—wait until no data hazards, then read operands (ID2)
  - All real dependencies (RAW hazards) resolved in this stage, since we wait for instructions to write back data.
  - No forwarding of data in this model!
Four Stages of Scoreboard Control

- **Execution**—operate on operands (EX)
  - The functional unit begins execution upon receiving operands. When the result is ready, it notifies the scoreboard that it has completed execution.

- **Write result**—finish execution (WB)
  - Stall until no WAR hazards with previous instructions:
    
    Example:  
    
    \[
    \begin{align*}
    \text{DIVD} & \quad F0, F2, F4 \\
    \text{ADDD} & \quad F10, F0, F8 \\
    \text{SUBD} & \quad F8, F8, F14
    \end{align*}
    \]
    
    CDC 6600 scoreboard would stall SUBD until ADDD reads operands.

Three Parts of the Scoreboard

- **Instruction status:**
  - Which of 4 steps the instruction is in

- **Functional unit status:**—Indicates the state of the functional unit (FU). 9 fields for each functional unit
  - Busy: Indicates whether the unit is busy or not
  - Op: Operation to perform in the unit (e.g., + or −)
  - Fi: Destination register
  - Fj,Fk: Source-register numbers
  - Qi,Qk: Functional units producing source registers Fj, Fk
  - Rj,Rk: Flags indicating when Fj, Fk are ready

- **Register result status**—Indicates which functional unit will write each register, if one exists. Blank when no pending instructions will write that register.

CDC 6600 Scoreboard

- **Speedup 1.7 from compiler; 2.5 by hand**
  - BUT slow memory (no cache) limits benefit

- **Limitations of 6600 scoreboard:**
  - No forwarding hardware
  - Limited to instructions in basic block (small window)
  - Small number of functional units (structural hazards), especially integer/load store units
  - Do not issue on structural hazards
  - Wait for WAR hazards
  - Prevent WAW hazards

Summary #1/2: Compiler techniques for parallelism

- **Loop unrolling**: Multiple iterations of loop in software:
  - Amortizes loop overhead over several iterations
  - Gives more opportunity for scheduling around stalls

- **Software Pipelining**: Take one instruction from each of several iterations of the loop
  - Software overlapping of loop iterations
  - Today will show hardware overlapping of loop iterations

- **Very Long Instruction Word machines (VLIW)**
  - Multiple operations coded in single, long instruction
    - Requires sophisticated compiler to decide which operations can be done in parallel
    - Trace scheduling: find common path and schedule code as if branches didn’t exist (+ add “fixup code”)

- **All of these require additional registers**
Summary #2/2

- **HW exploiting ILP**
  - Works when can’t know dependence at compile time.
  - Code for one machine runs well on another

- **Key idea of Scoreboard:** Allow instructions behind stall to proceed (Decode => Issue instr & read operands)
  - Enables out-of-order execution => out-of-order completion
  - ID stage checked both for structural & data dependencies
  - Original version didn’t handle forwarding.
  - No automatic register renaming