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Homework Quiz (HW #6)

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CS152 Computer Architecture and Engineering

This quiz covers one of the problems from homework #6.
Good Luck!

Your Name:	**Solutions**
SID Number:	
Discussion Section:	

Total:	**10/10**

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Cache organization

Your company has an application that must be run as fast as possible. The hardware division of your company has come up with three separate first-level cache configurations:

- *Machine I:* Direct-mapped with one-word blocks
- *Machine II:* Direct-mapped with four-word blocks
- *Machine III:* Two-way set associative with four-word blocks

For these machines, the cache fill penalty is 4 cycles + 1 cycle for each word.

You did some experiments and measured the following instruction mix for the application:

Branch: 16%, Load: 15%, Store: 10%, Float Insts: 20%, Integer: 39%

Further, through a hardware cache monitor, you measured the following miss rates:

- *Machine I:* Instruction miss rate: 4%; Data miss rate: 20%
- *Machine II:* Instruction miss rate: 2%; Data miss rate: 16%
- *Machine III:* Instruction miss rate: 1.5%; Data miss rate: 14%

Finally, the total CPI measured with Machine I is 3.0.

1. Which of these machines spends the most time waiting for memory? Justify your answer:
Solution:
Data reference: *Load = 15% = 0.15*
Store = 10% = 0.1
Total = 0.15 + 0.1 = 0.25
Instruction Reference: 1, because 1 instruction is fetched every cycle

Machine I: time waiting for memory = 5(0.04*1+ (0.1 + 0.15)*0.2) = 0.45*
5 = fill penalty for 1 word block
Machine II: time waiting for memory = 8(0.02*1+ (0.1 + 0.15)*0.16) = 0.48*
Machine III: time waiting for memory = 8(0.015*1+ (0.1 + 0.15)*0.14) = 0.40*
8 = fill penalty for 4 word block

Thus machine II spend the most time waiting for memory.

2. Suppose we increase the associativity of Cache III (keeping the block-size constant). In this new configuration, the instruction miss rate goes to zero. Further, we measure a total CPI of **2.71.** What is the data miss rate?
Solution:
Base CPI without memory stalls = 3.0 – 0.45 = 2.55 ← This number is not 1 because it includes data dependent stalls. It is the same for all three machines.

Thus, 2.71 – 2.55 = 0.16 of the CPI is waiting for memory. This number is only for data miss since instruction miss rate goes to zero.

0.16 = 8(0.1 + 0.15)*Data Miss Rate ➔ Data Miss Rate = 8%*