University of California, Berkeley
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Computer Science Division — EECS

Spring 1999 John Kubiatowicz

Homework Quiz (HW #5)

April 5, 1999
CS152 Computer Architecture and Engineering

This quiz covers one of the problems from homework #5.
Good Luck!

Your Name:	
SID Number:	
Discussion Section:	

Total:	

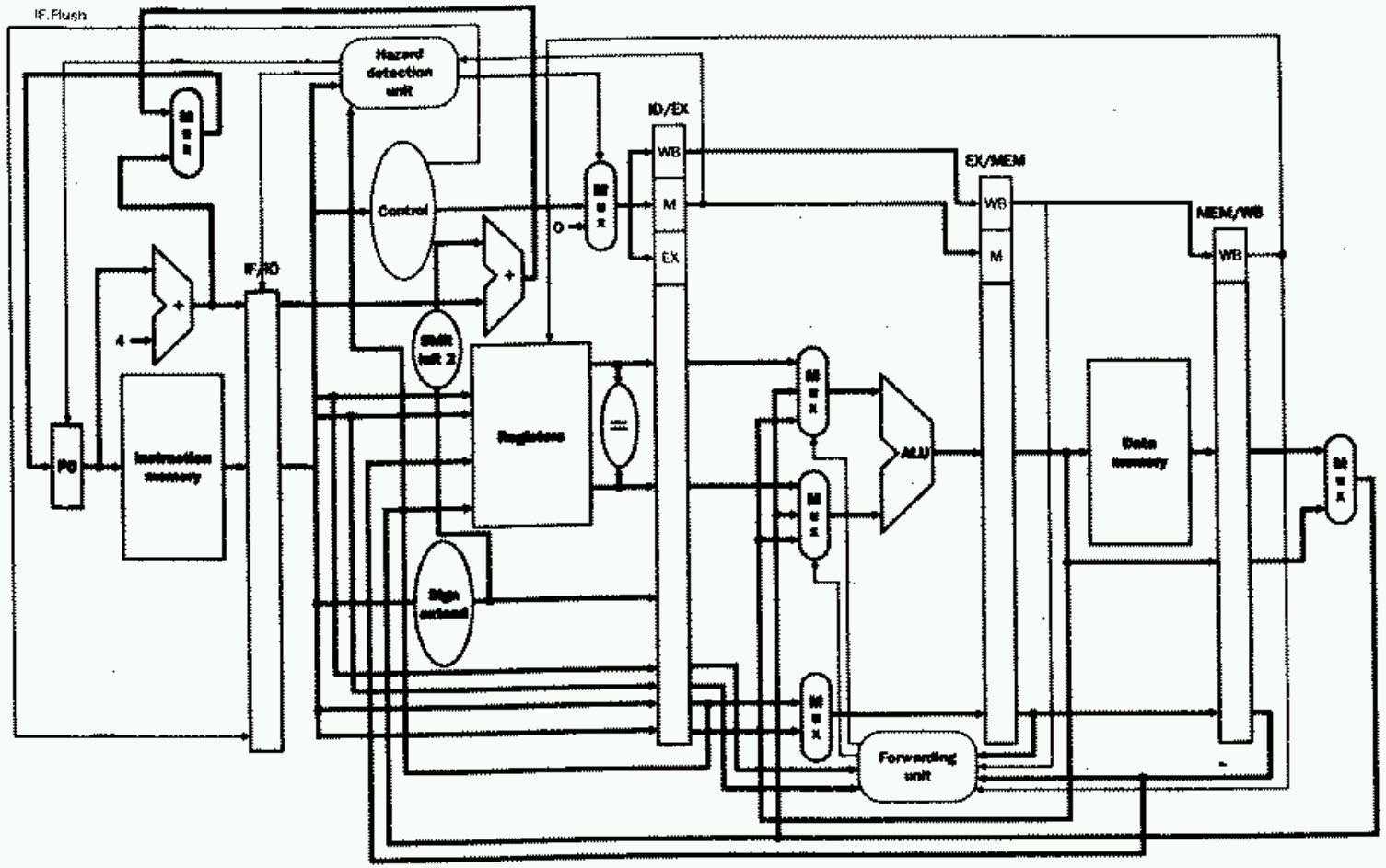

FIGURE 6.51 Datapath for branch, including hardware to flush the instruction that follows the branch. This optimization moves the branch decision from the fourth pipeline stage to the second; only one instruction that follows the branch will be in the pipe at that time. The control lines IF.Flush turns the fetched instruction into a nop by zeroing the IF/ID pipeline register. Although the flush line is shown coming from the control unit in this figure, in reality it comes from hardware that determines if a branch is taken, labeled with an equal sign to the right of the registers in the ID stage.

In problem 6.26, you were asked to consider a pipeline *which does not support a delayed branch*. Figure 6.51 from one of the printings of the book is reproduced on the previous page.

1. In this datapath, how many instructions must be "flushed" out of the pipeline when a branch is taken? Explain.

2. What must be in the "Control" oval in order to support flushing (i.e. when does it decide to assert IF.Flush)? What exactly does the "IF.Flush" signal do?

3. Consider the following instruction sequence:

```
sub $2, $4, $5
beq $2, $3, somewhere
```

   Why doesn't this code sequence work properly on this hardware (this is a bug in the book!)?

4. Can you fix this problem without increasing the number of instructions flushed on a taken branch? If so, how? If not, why not? You can use space on the back of this sheet if necessary.